Slim NoC: A Low-Diameter On-Chip Network Topology for High Energy Efficiency and Scalability

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SAFARI

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PITTSBURGH PENNSYLVANIA 1900

MASSIVELY PARALLEL MANYCORES

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SW26010: 260 cores

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PEZY-SC2: 2048 cores

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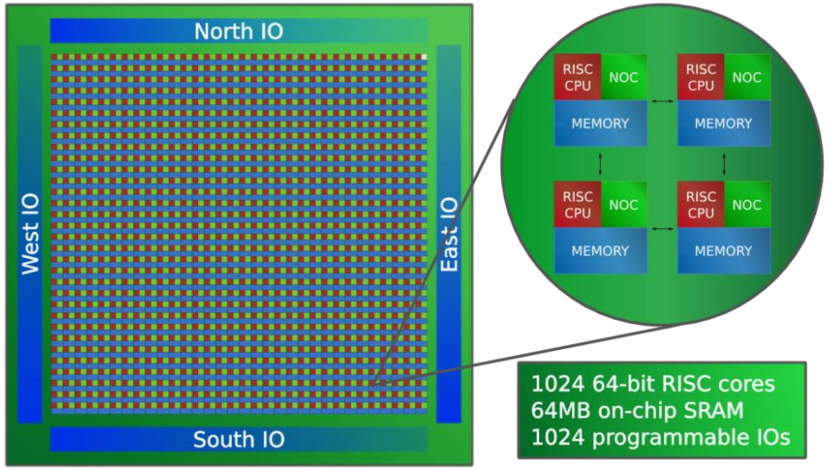

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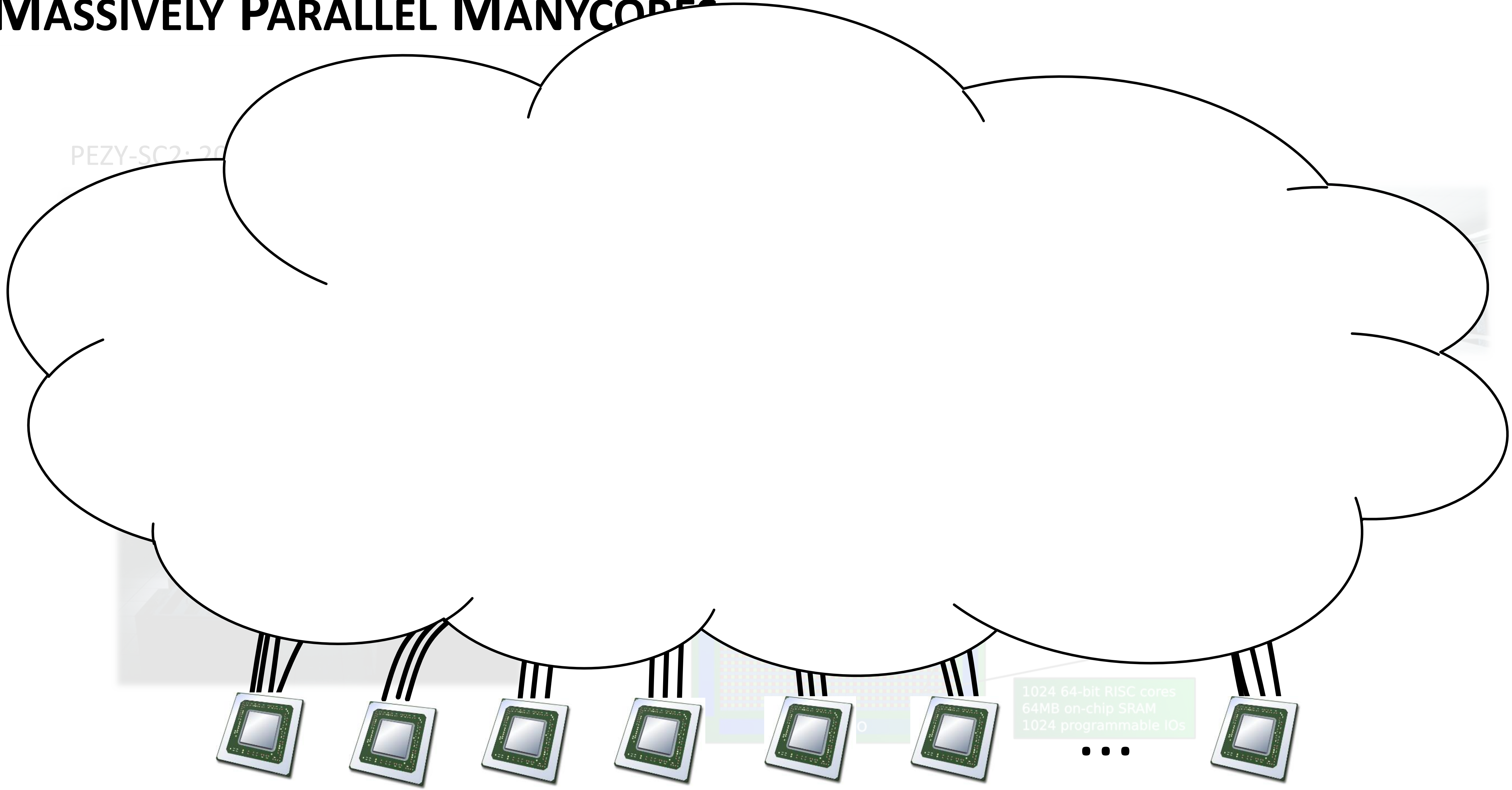

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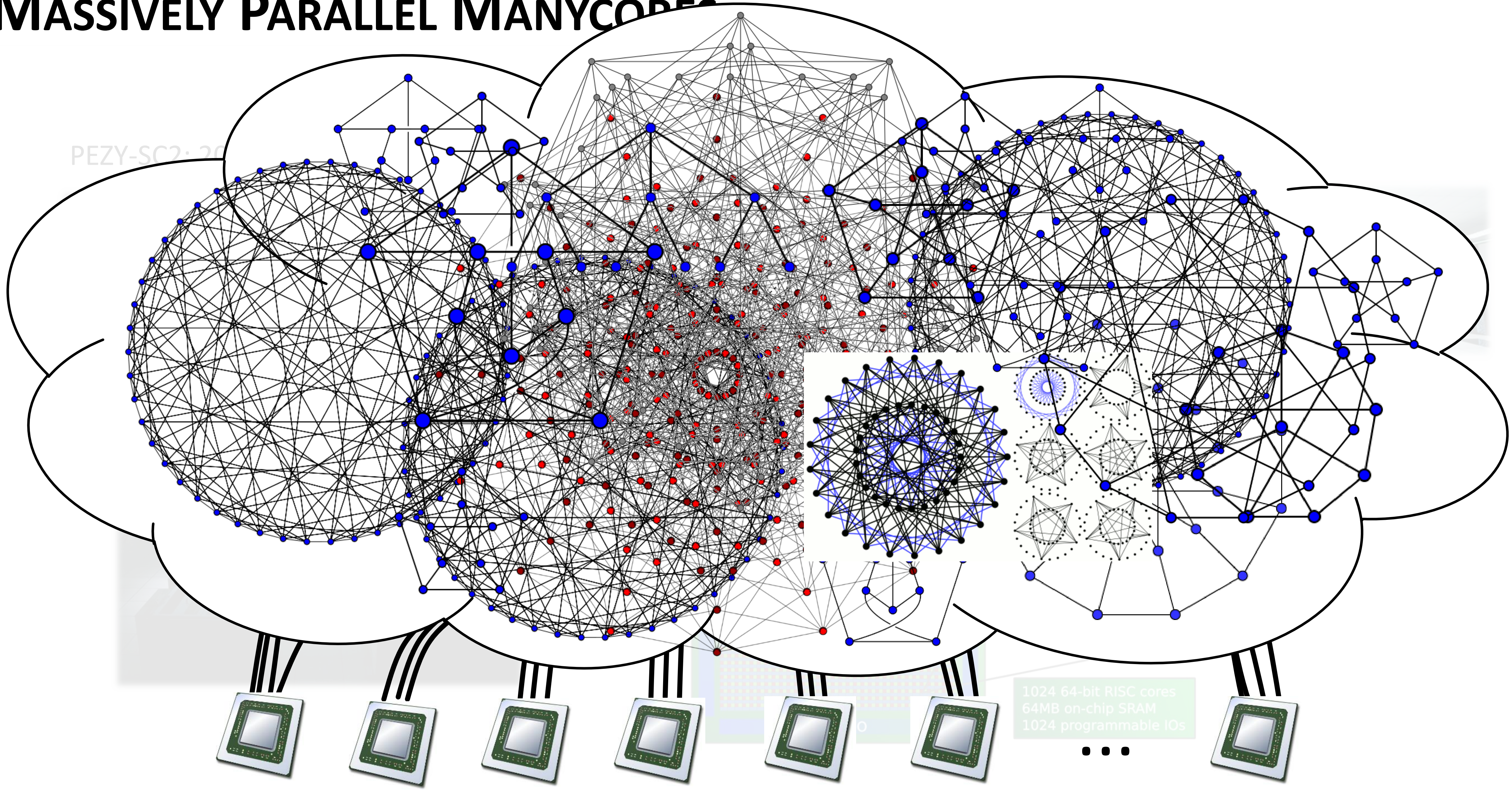

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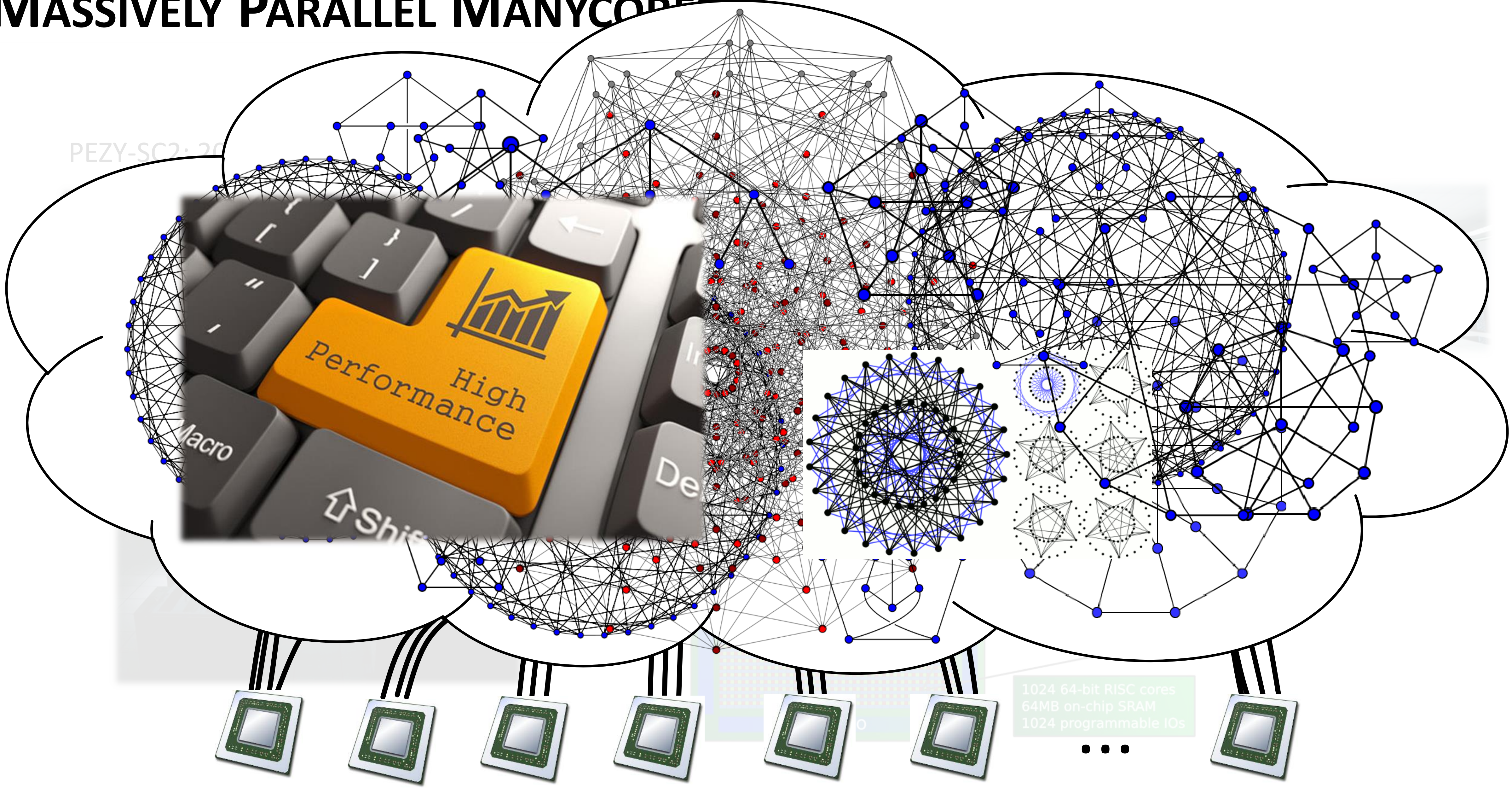

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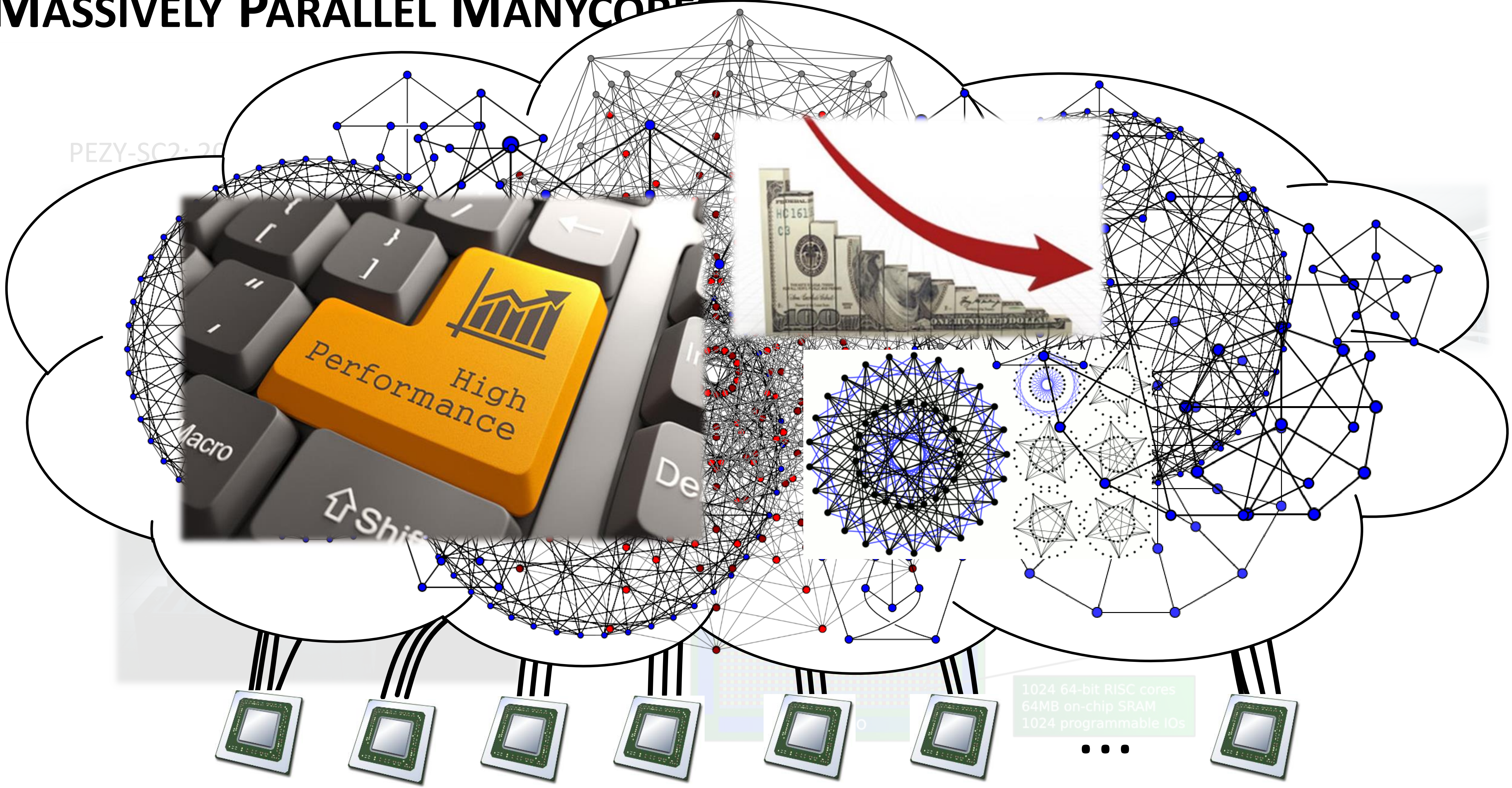

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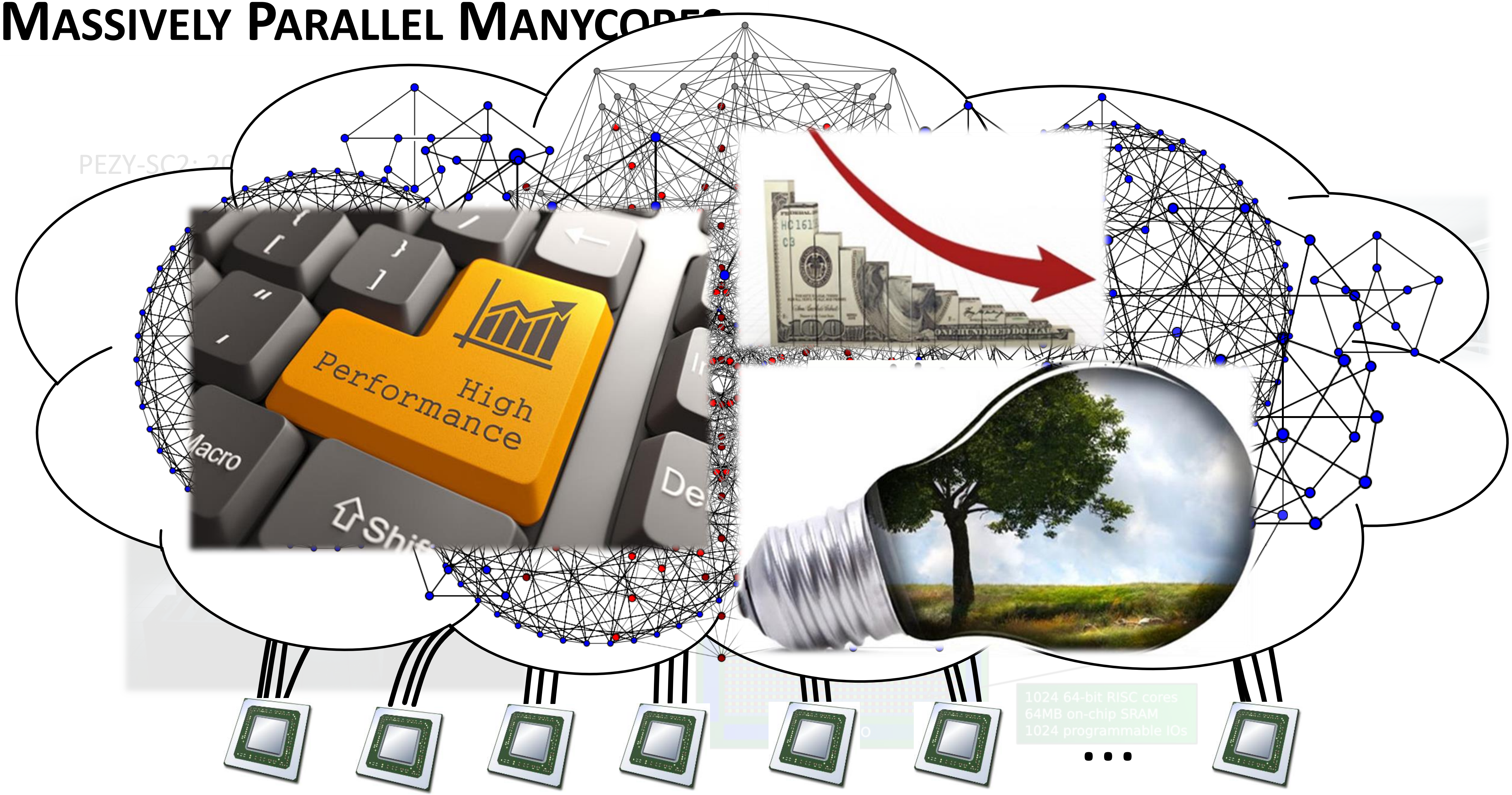

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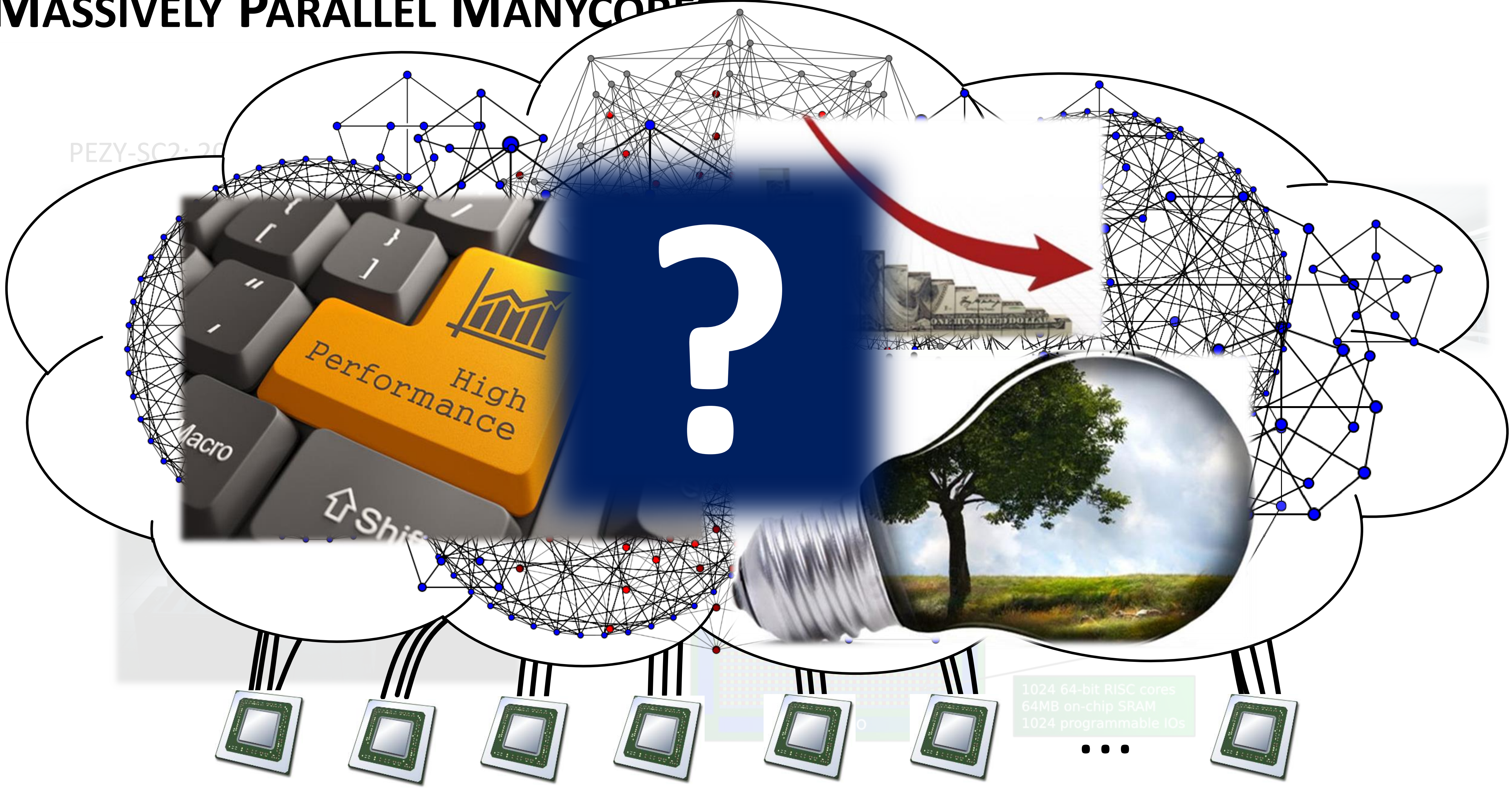
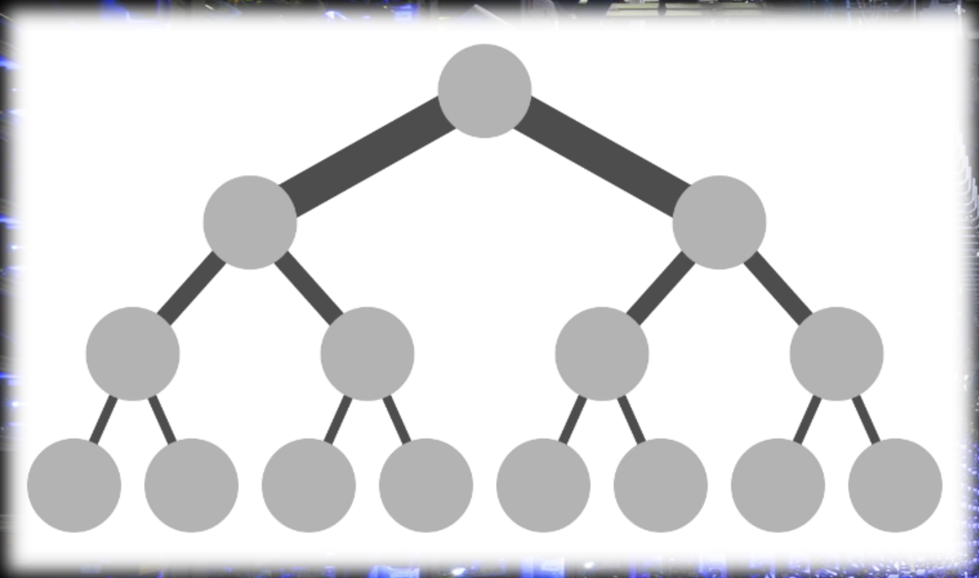
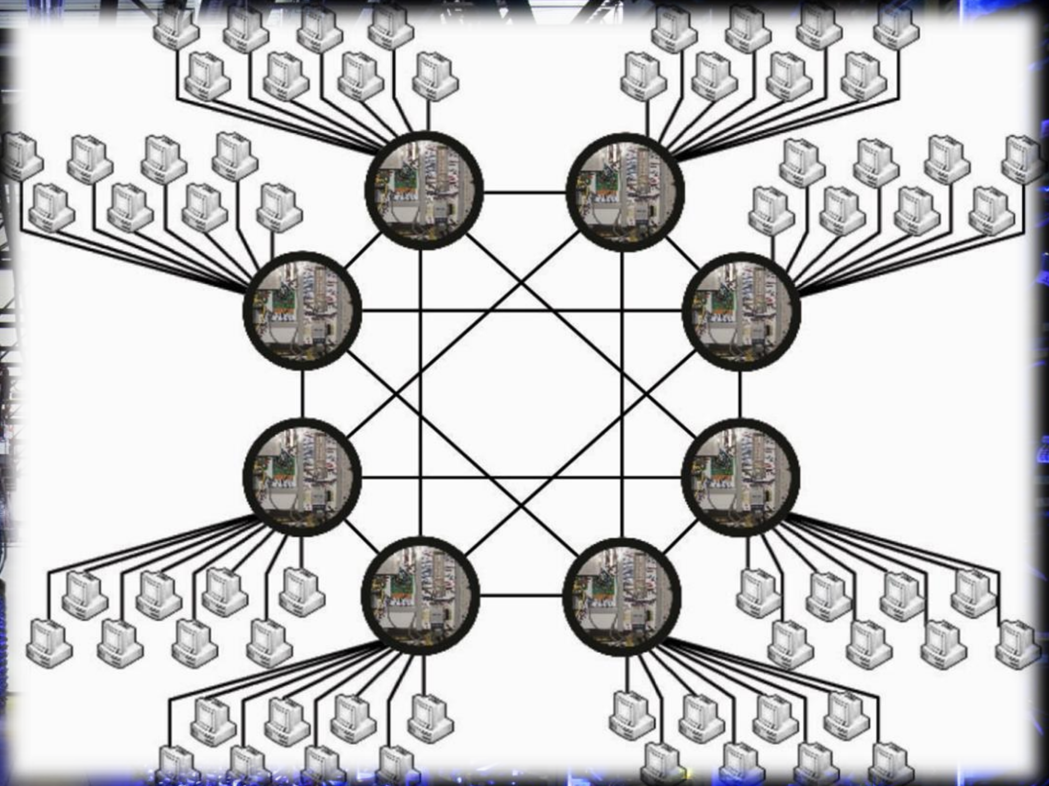
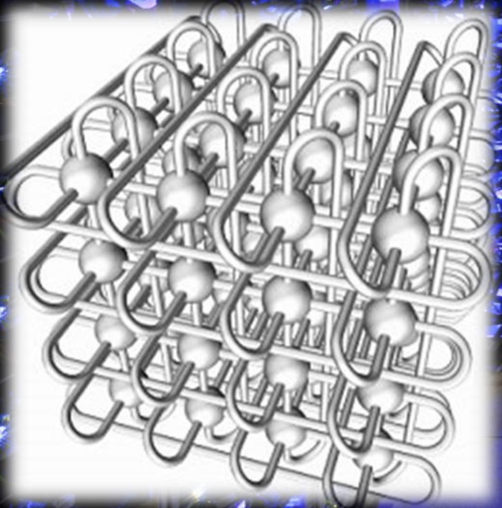


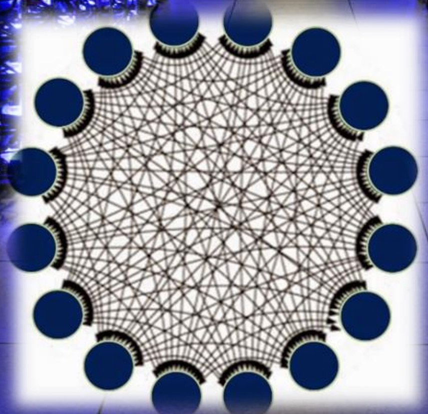
NETWORKS IN COMPUTE CLUSTERS

Networks in Compute Clusters





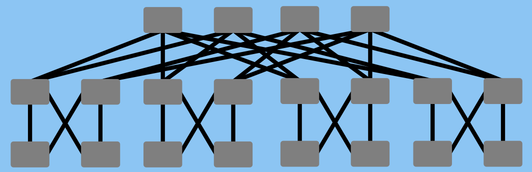




Dragonfly, Slim Fly

DRAGONFLY, SLIM FLY

Fat tree [1]



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TSUBAME2.0

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DRAGONFLY, SLIM FLY

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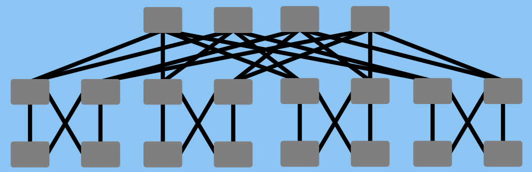

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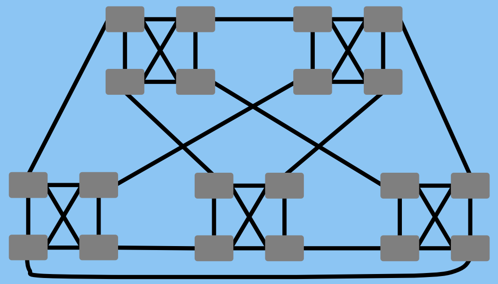

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Cray Cascade

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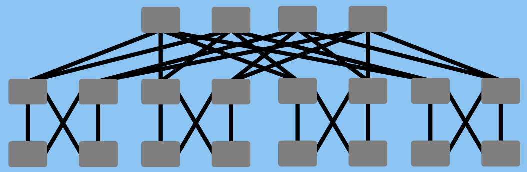

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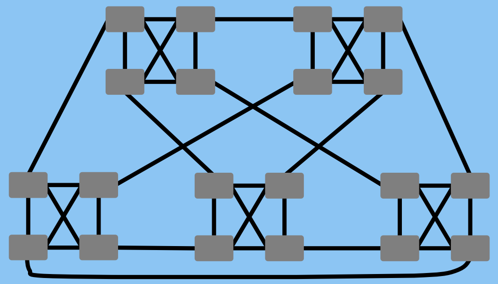

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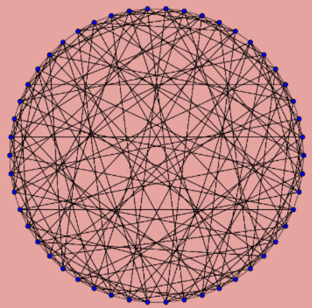
Slim Fly [3] based on the Hoffman-Singleton Graph [4]:

> ~50% fewer routers than Fat tree

> ~30% fewer cables than Fat tree



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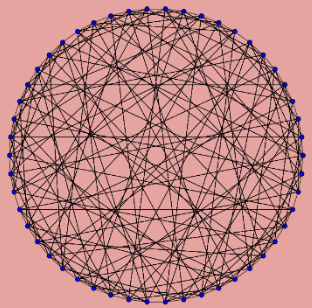

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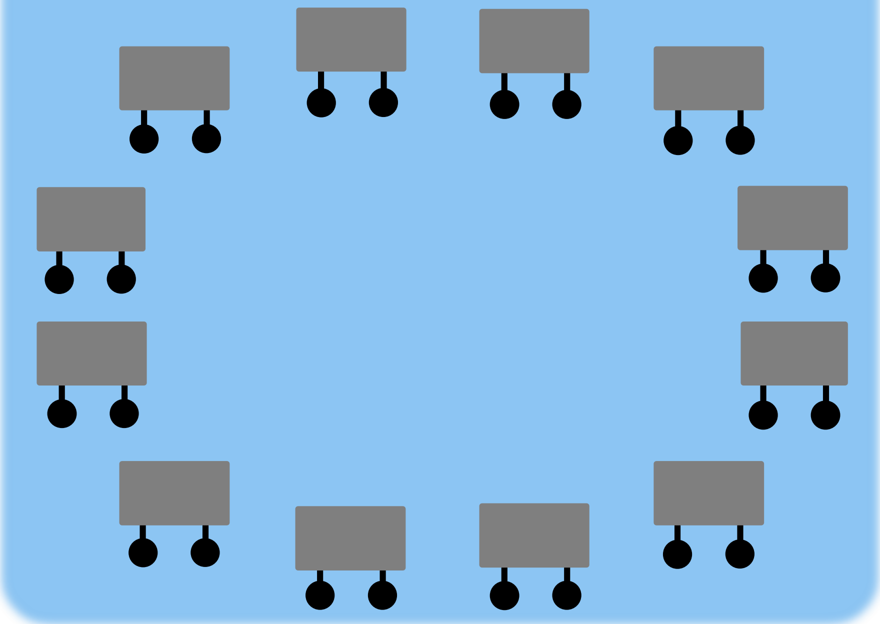

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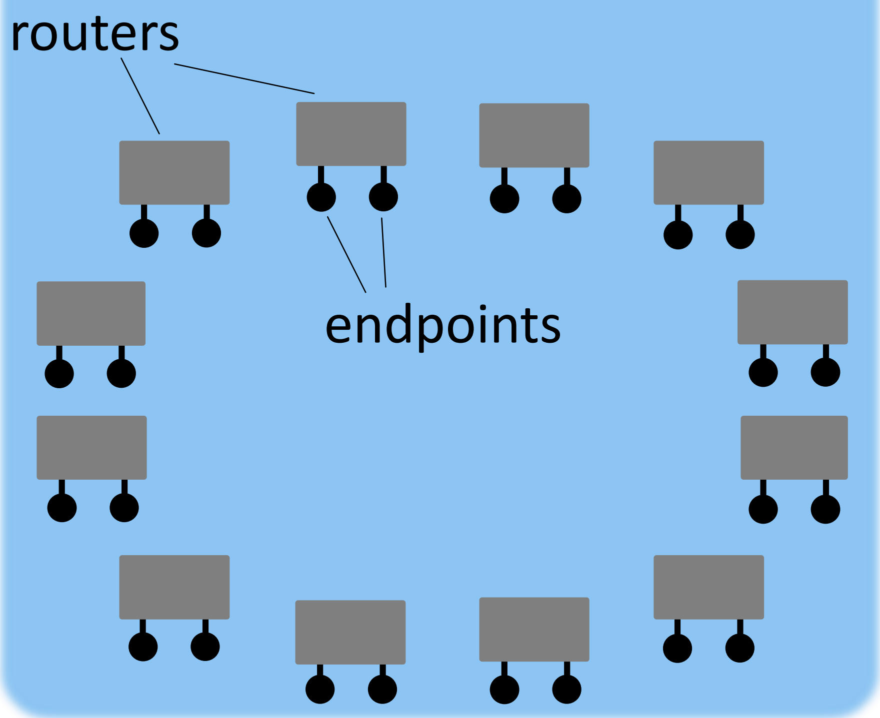

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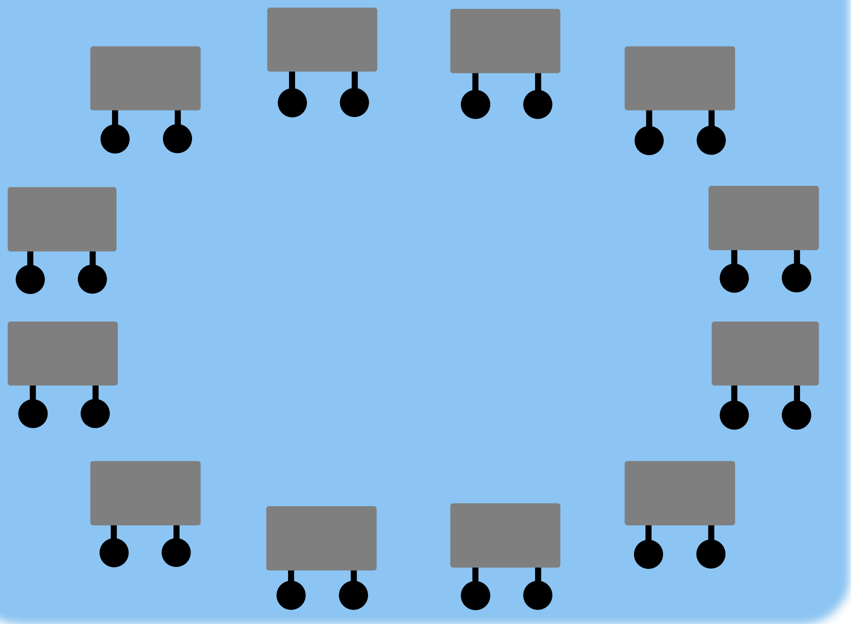

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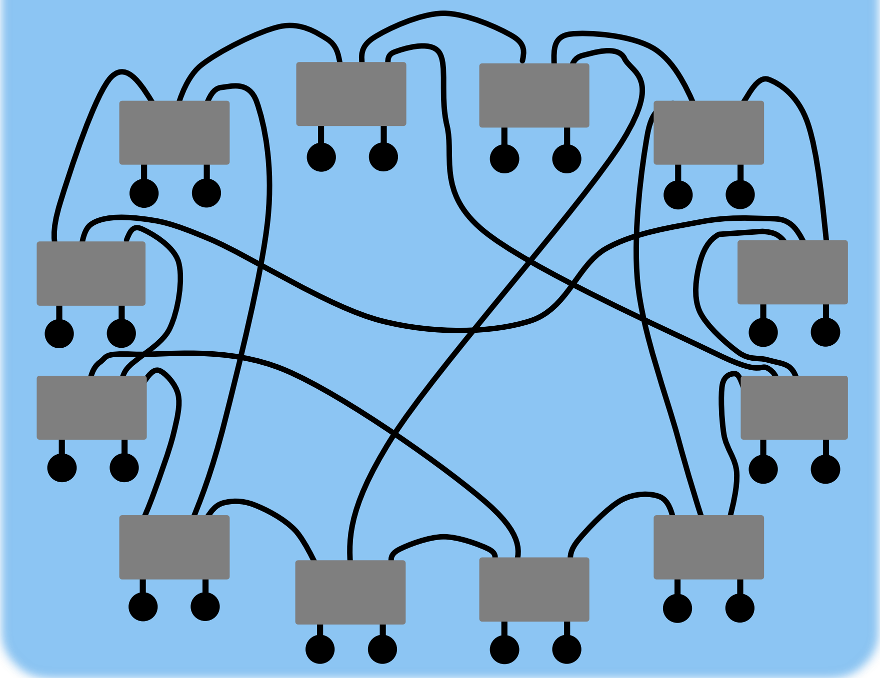

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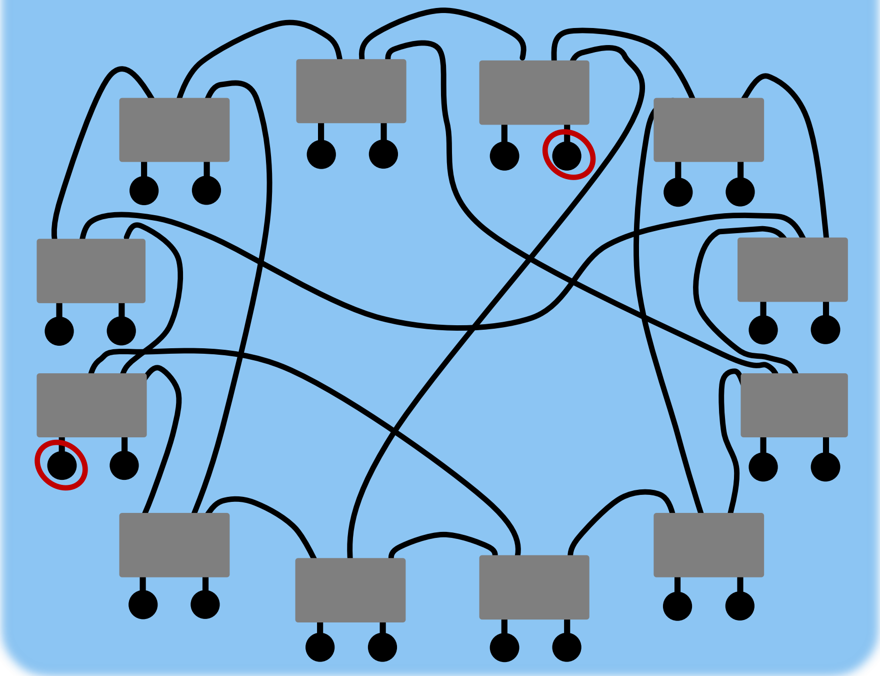

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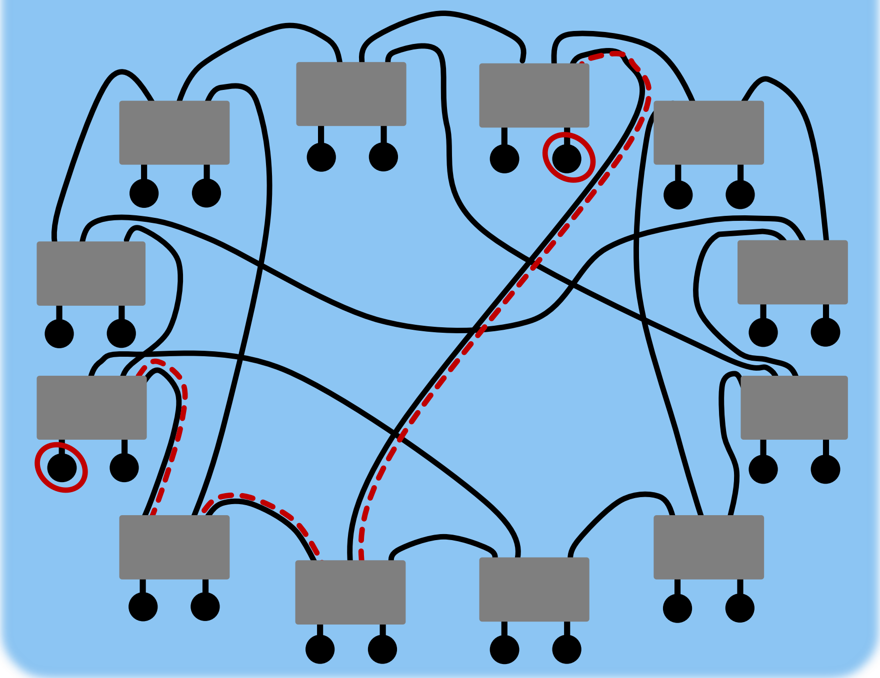

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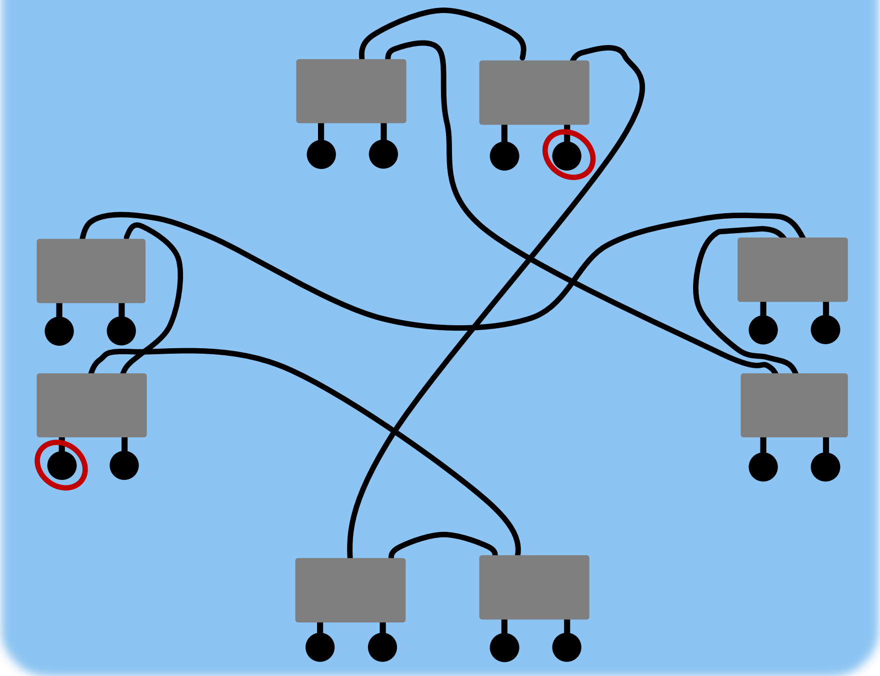

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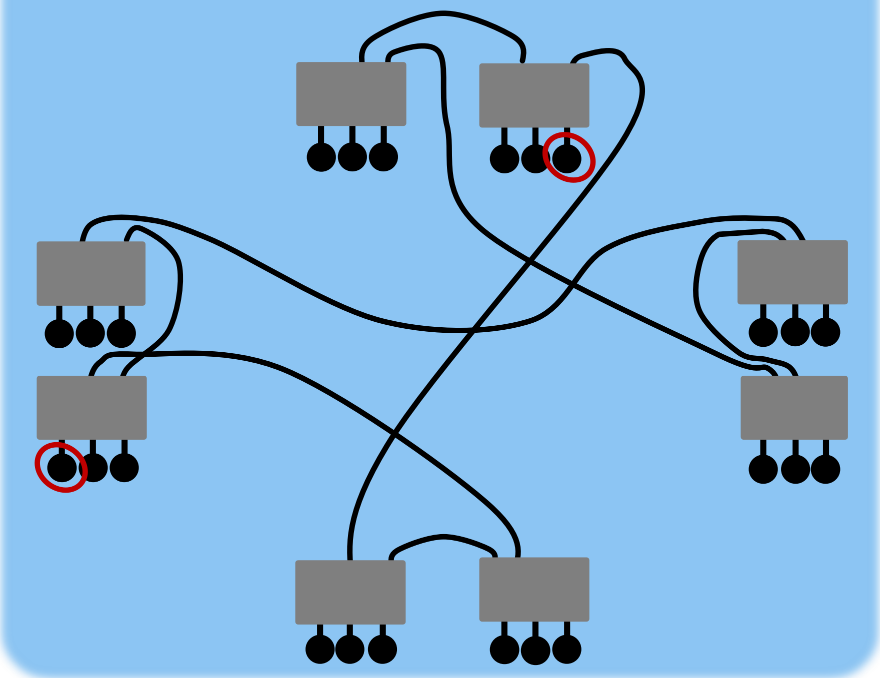

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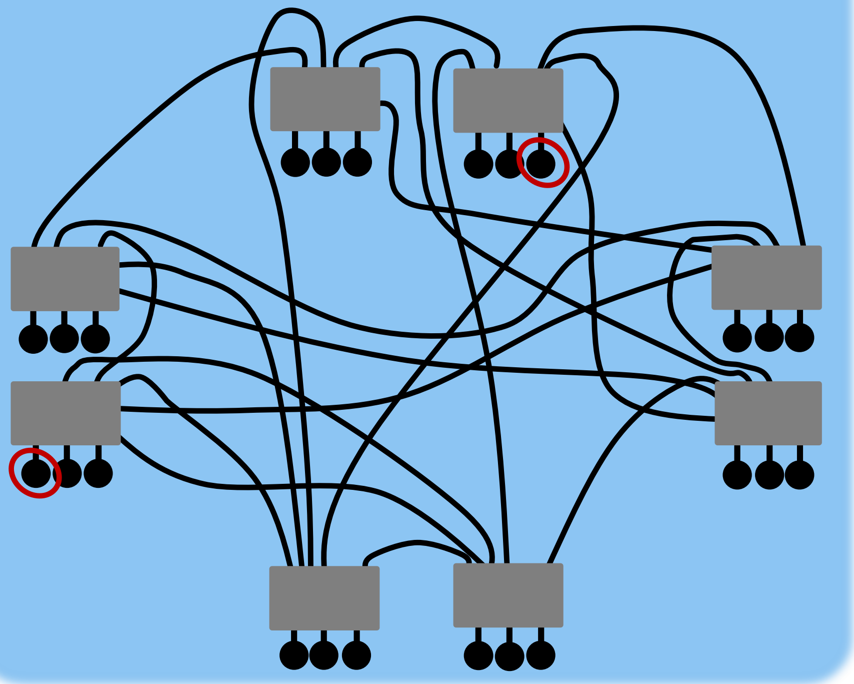

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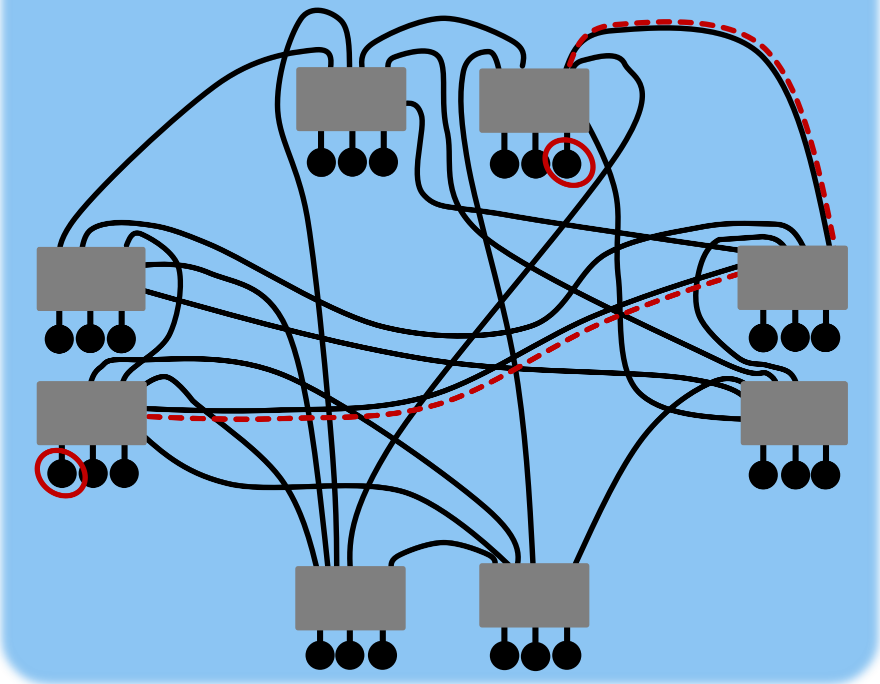

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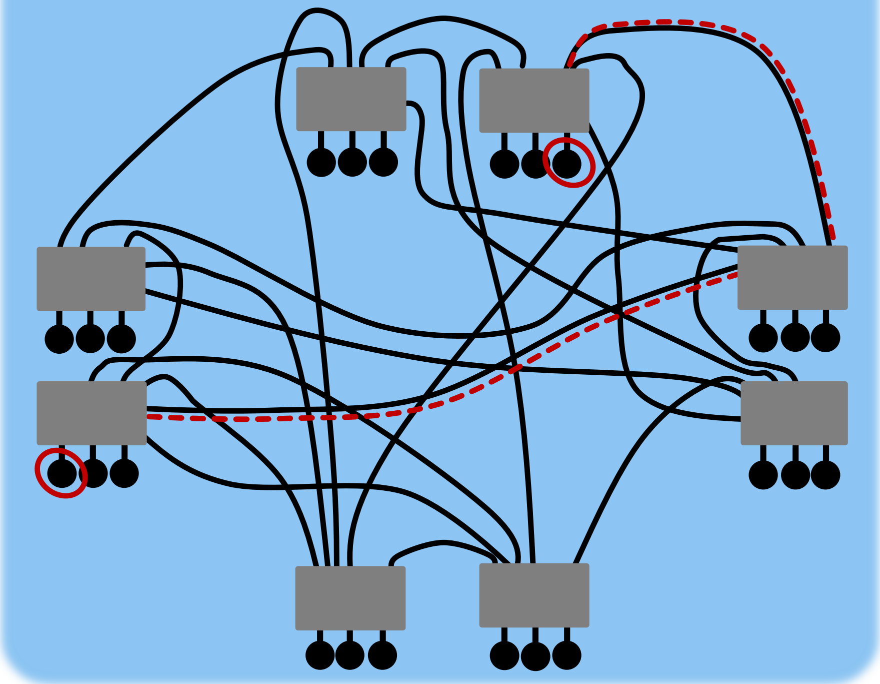

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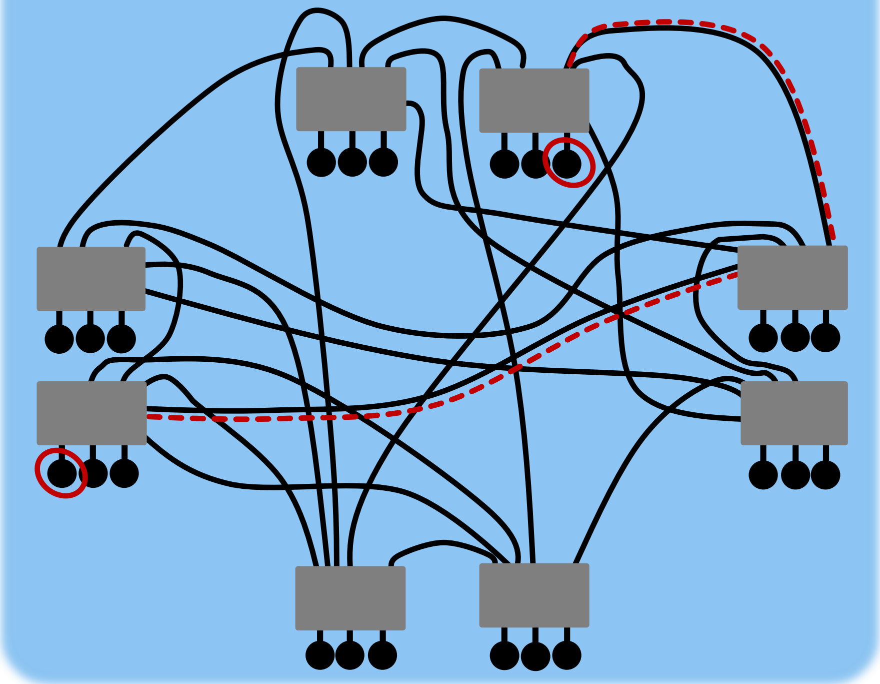

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Optimize towards the Moore Bound [1]: the upper bound on the *number of vertices* in a graph with given *diameter D* and *radix k*.

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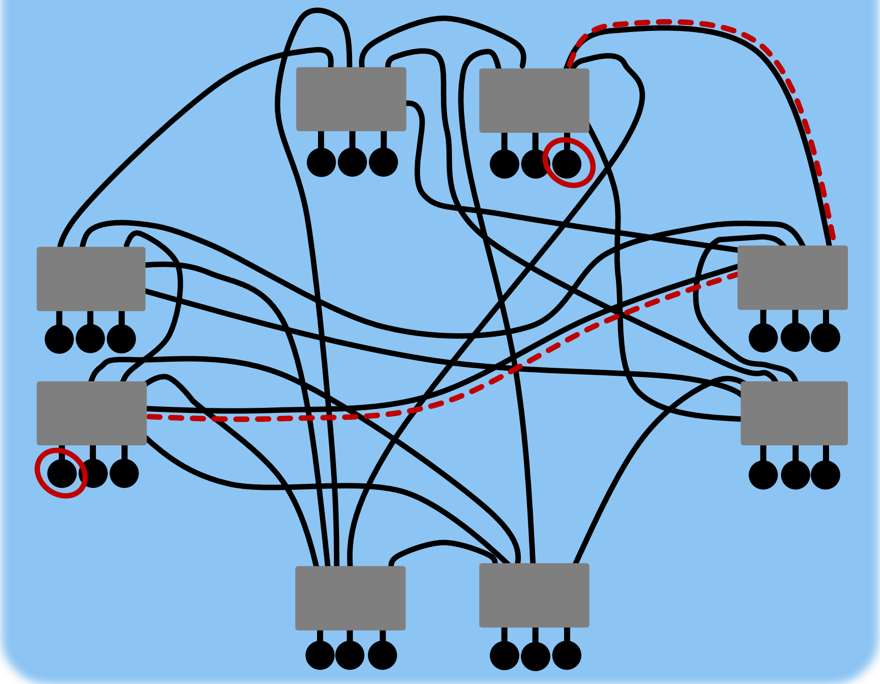

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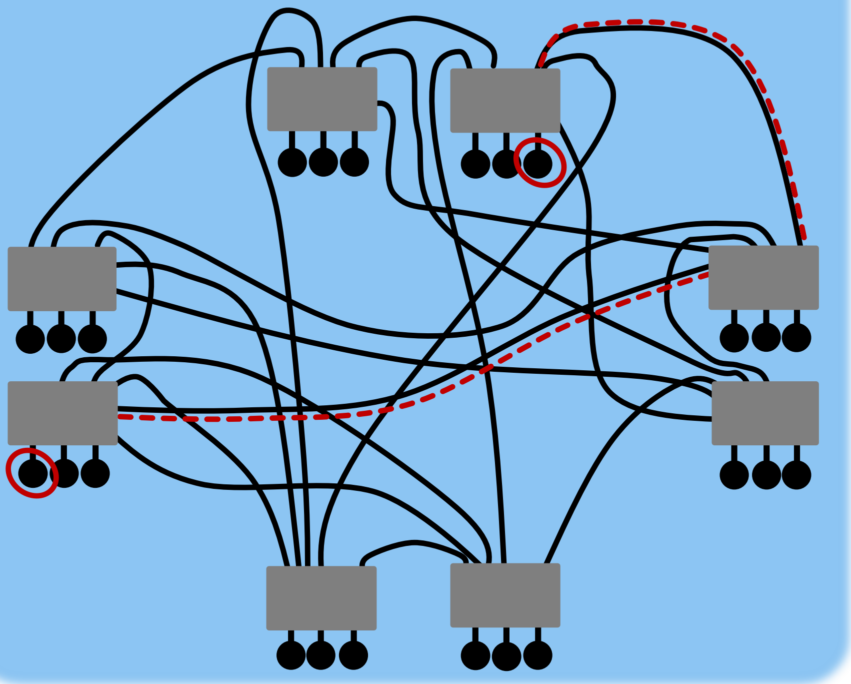

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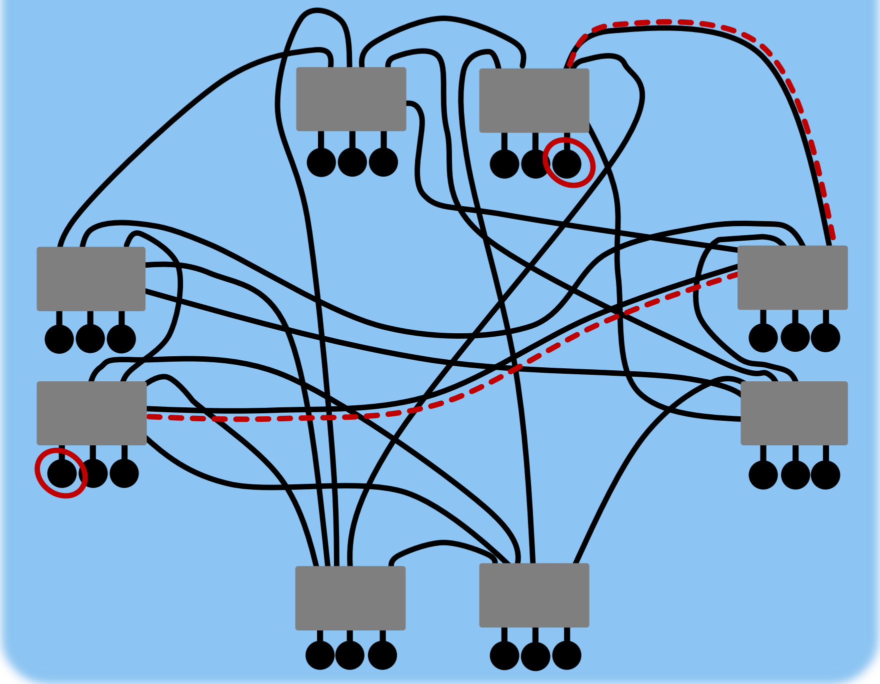

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$$MooreBound(D, k) = 1$$

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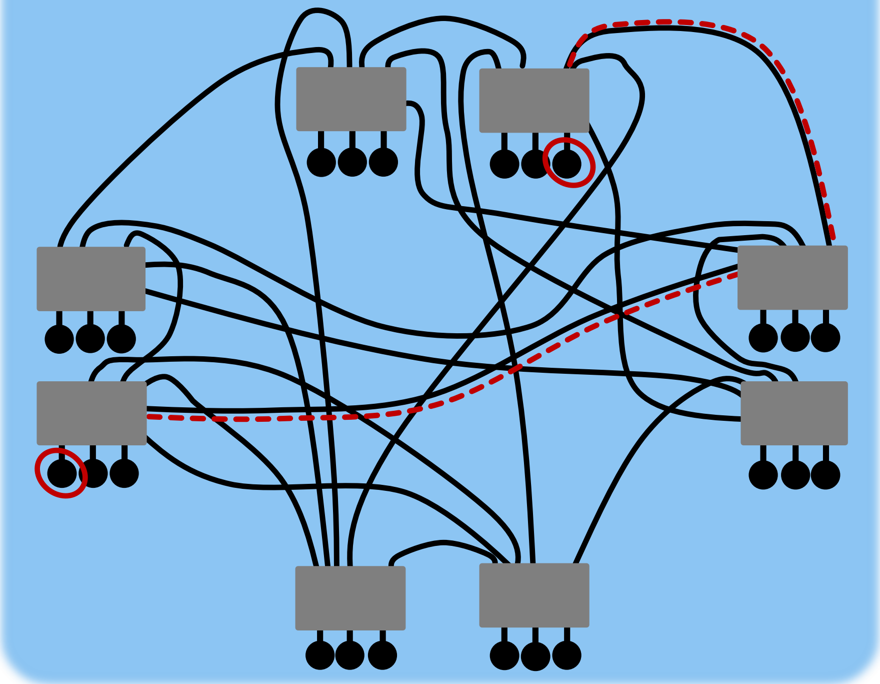

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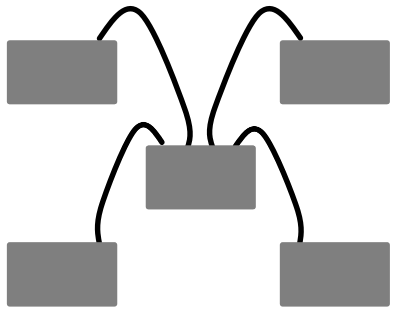

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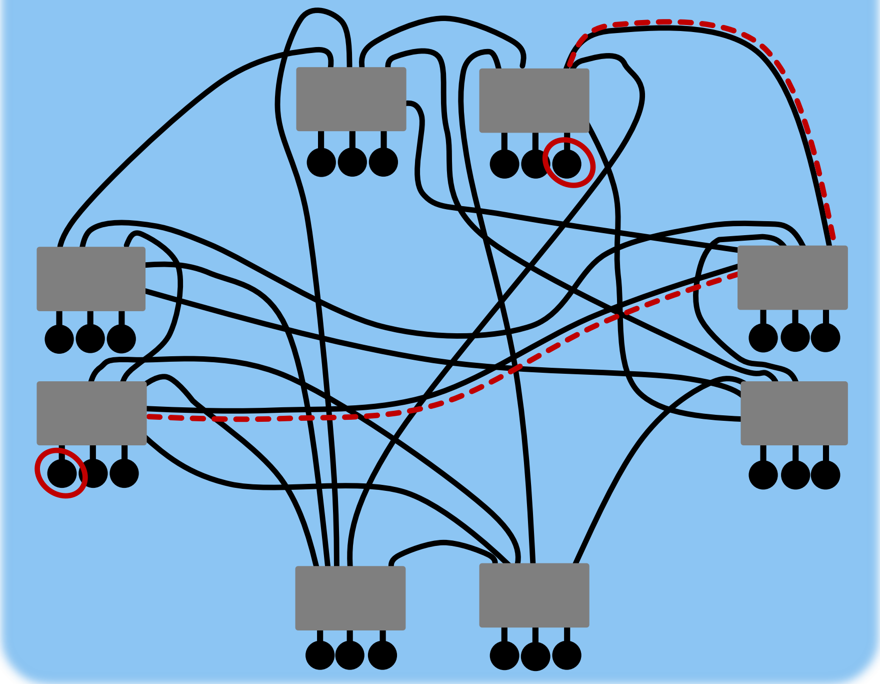

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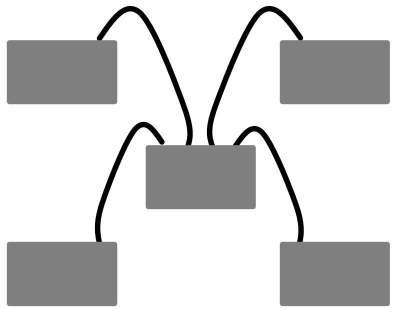
$$MooreBound(D, k) = 1 \; + k$$



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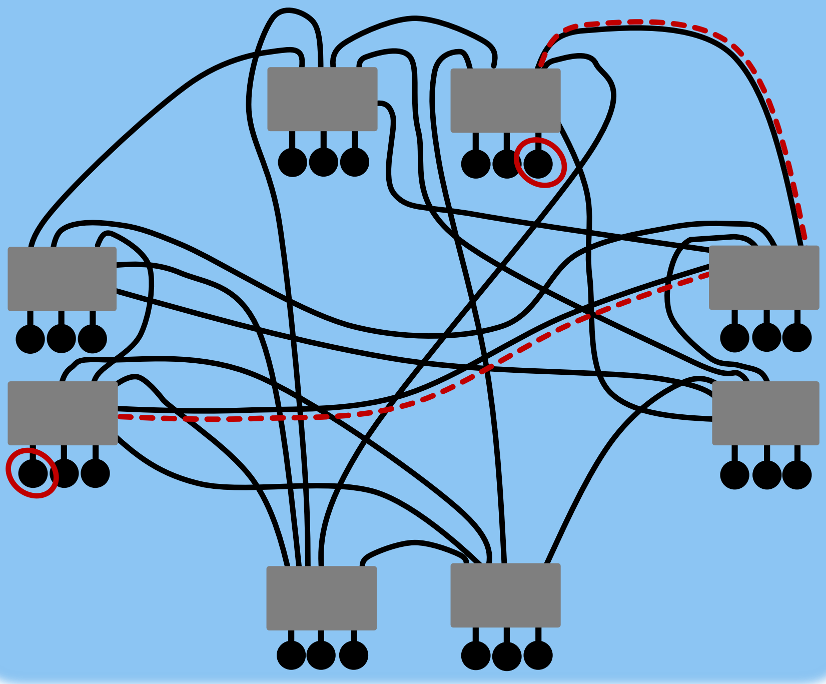

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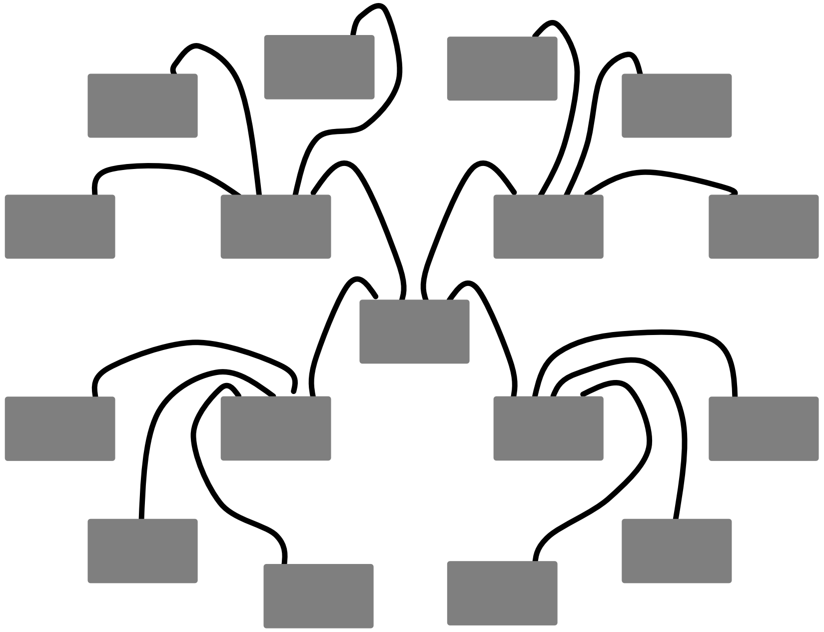

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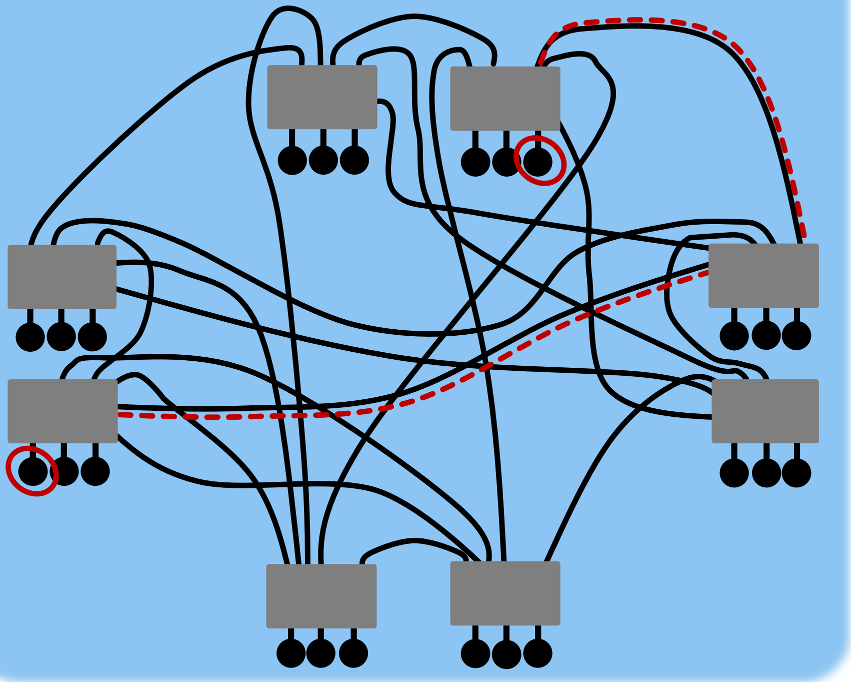

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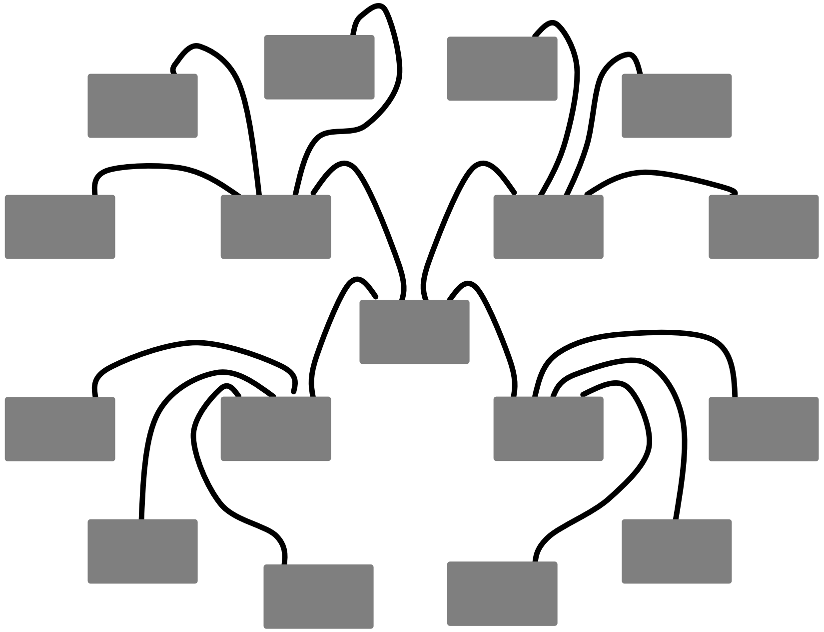

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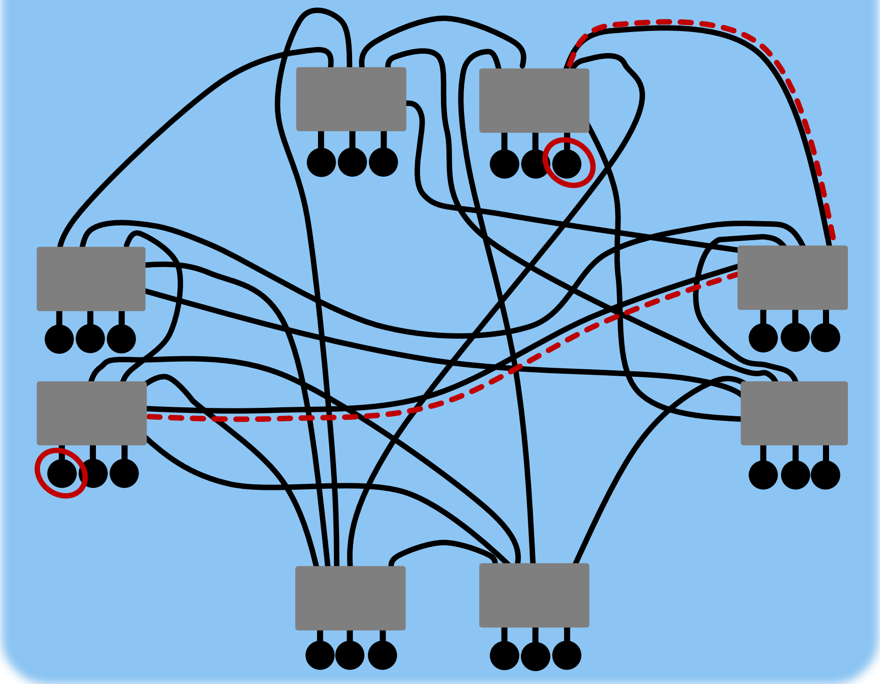

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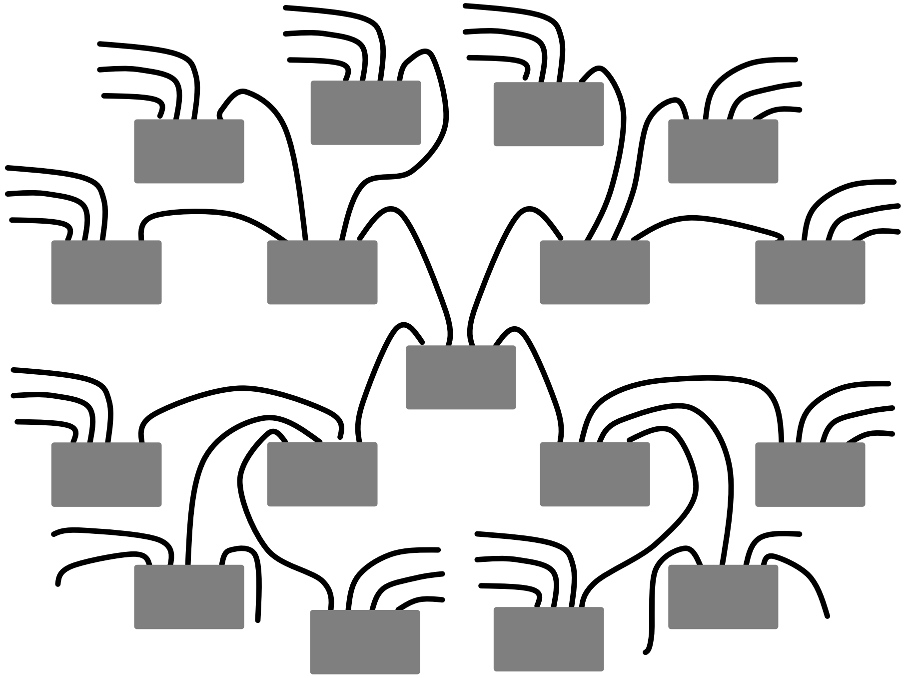

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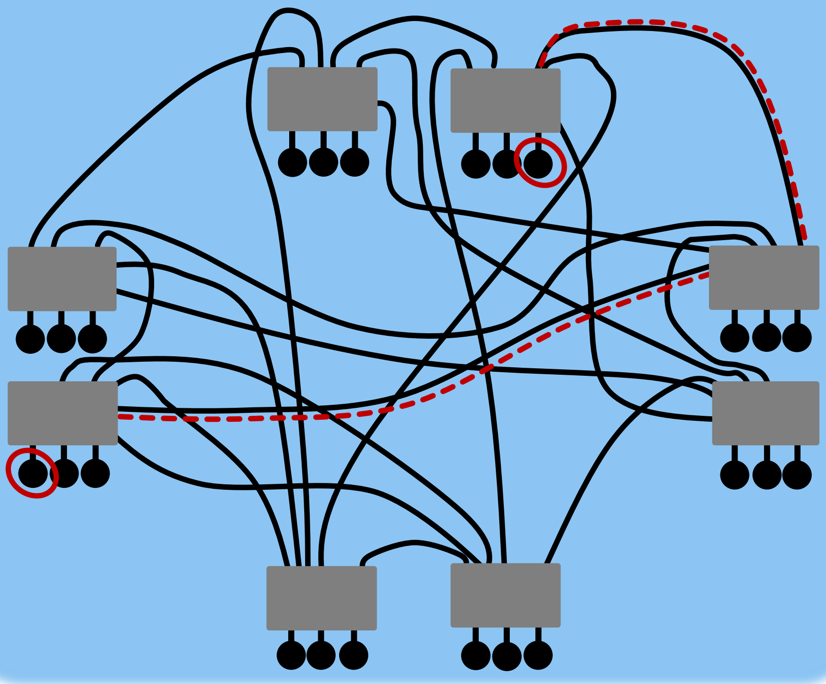

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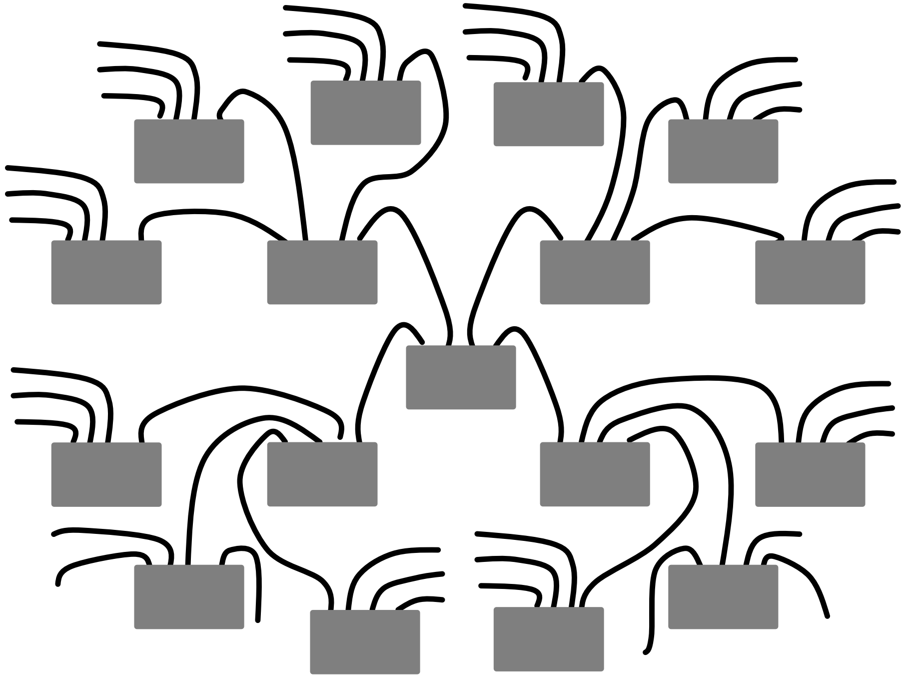

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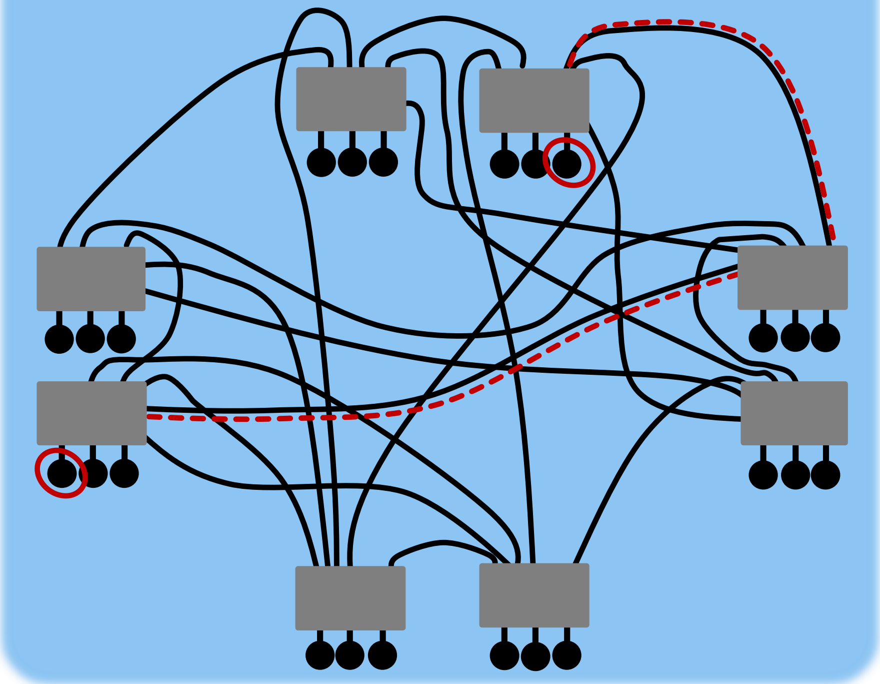

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Thus, Slim Fly ensures the lowest radix (port count) for a given node count and for a fixed diameter... Sounds ideal for an on-chip setting?

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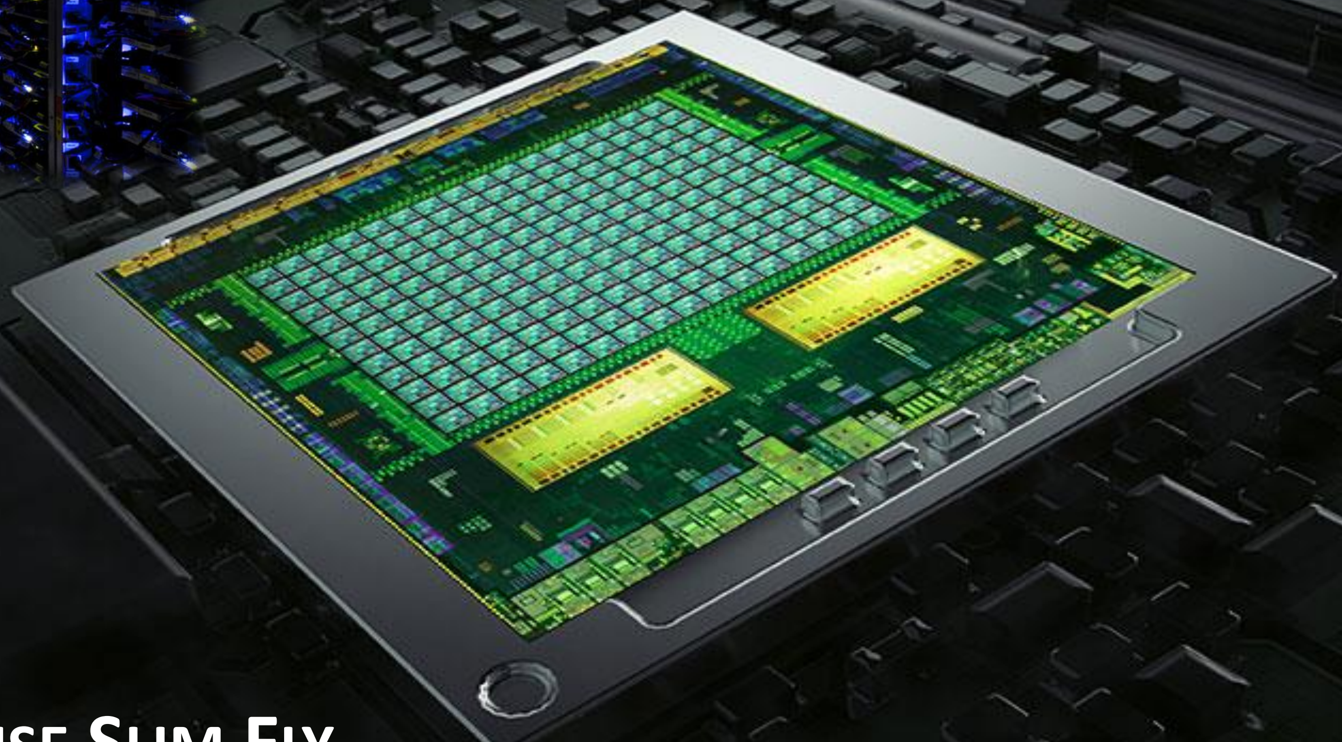

Why not just use Slim Fly as an on-chip network?

Slim Fly on Chip – First Attempt
Structure Intuition

- Example design for *diameter* = 2

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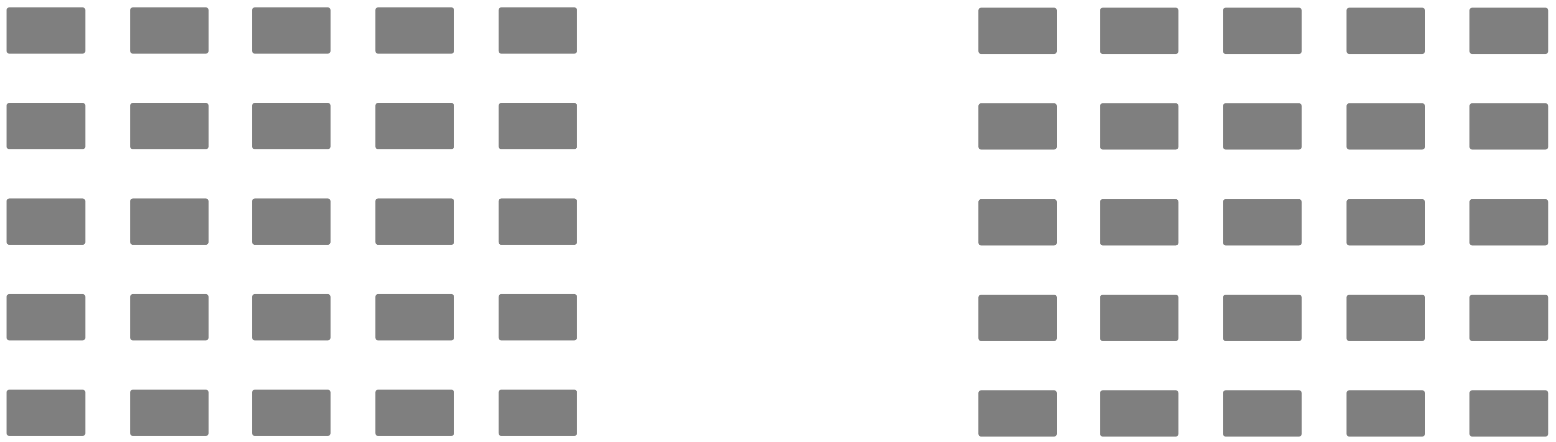

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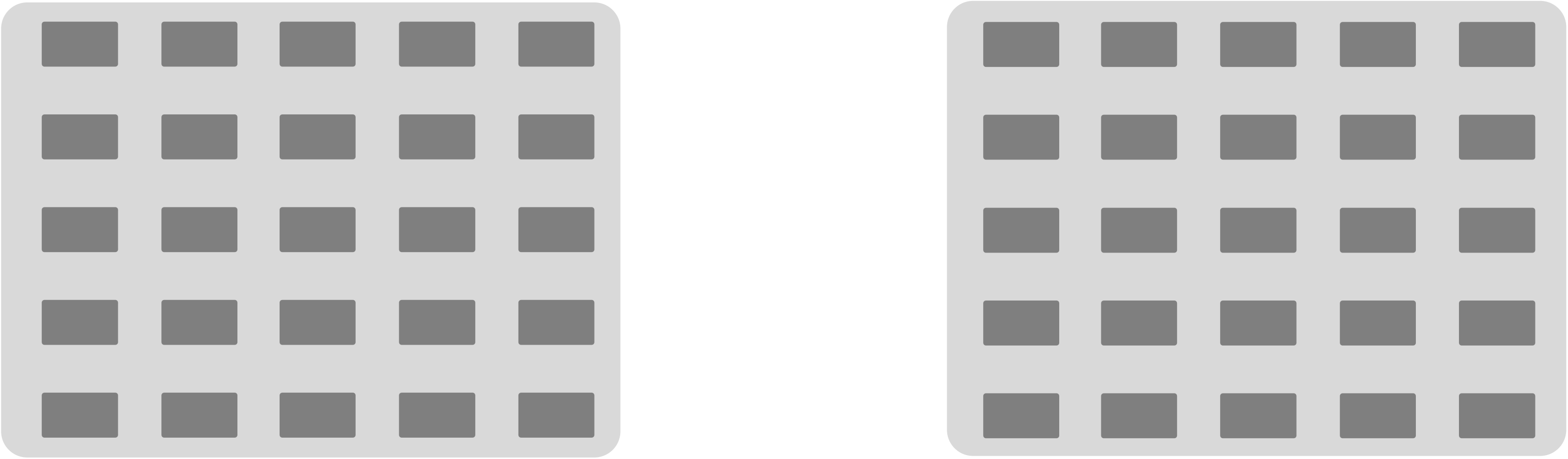
A subgraph with
identical groups of routers



Slim Fly on Chip – First Attempt
Structure Intuition

- Example design for *diameter* = 2

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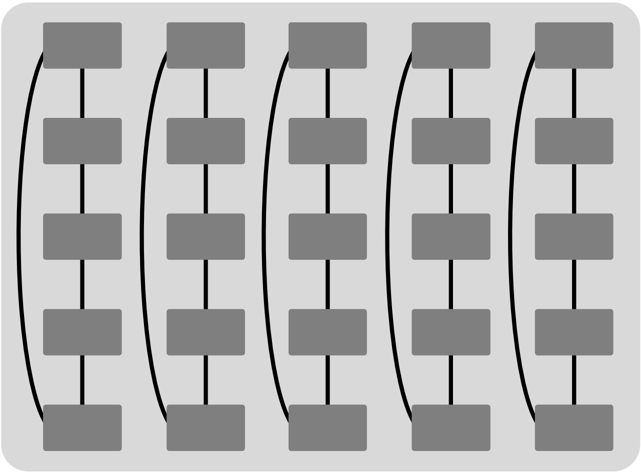

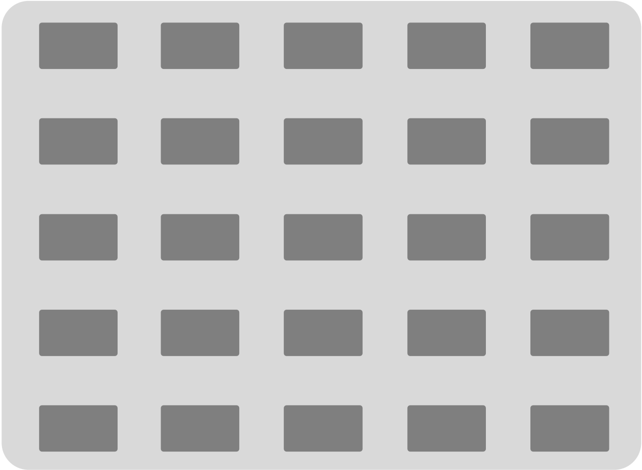

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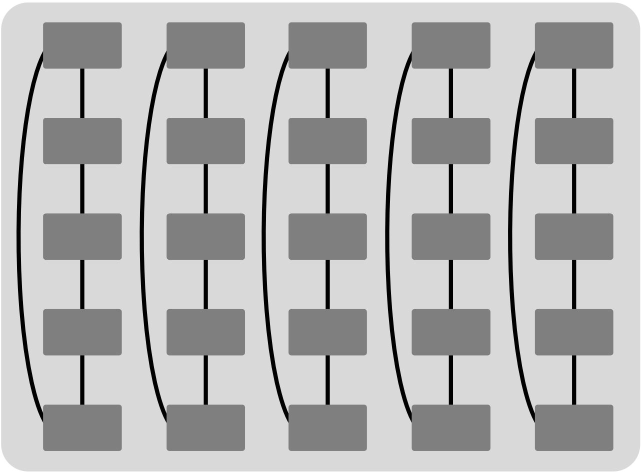

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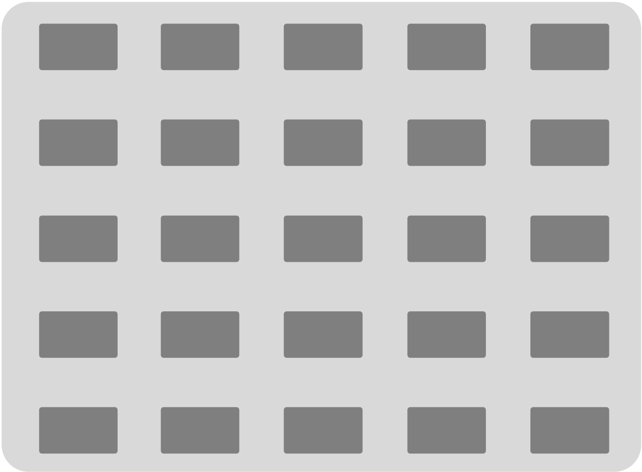

SLIM FLY ON CHIP – FIRST ATTEMPT
STRUCTURE INTUITION

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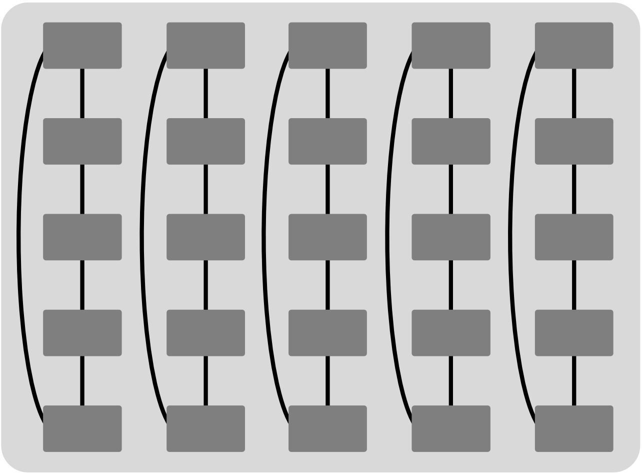

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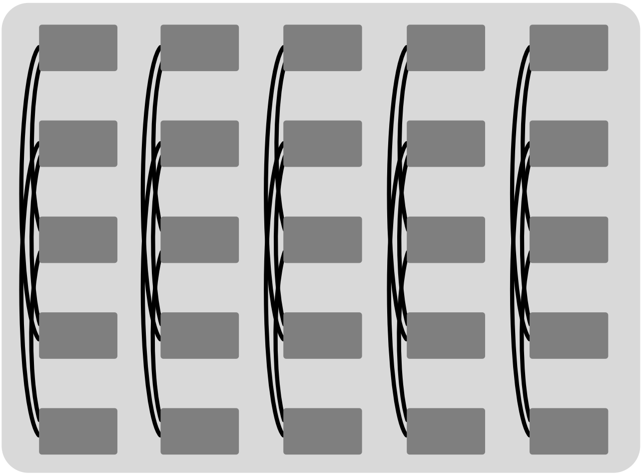

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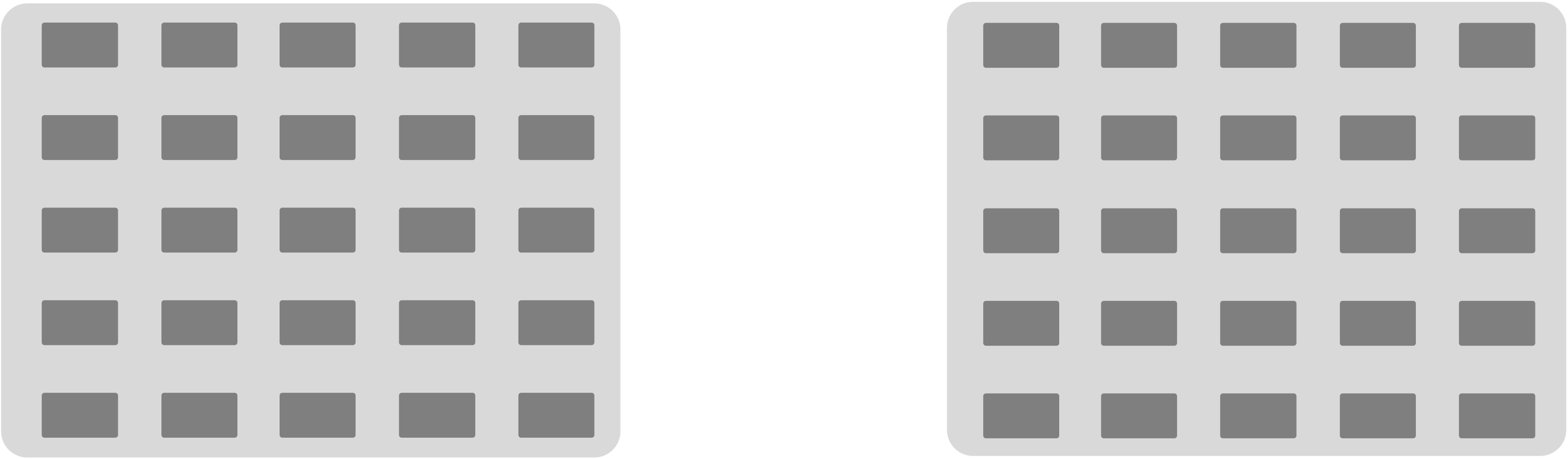

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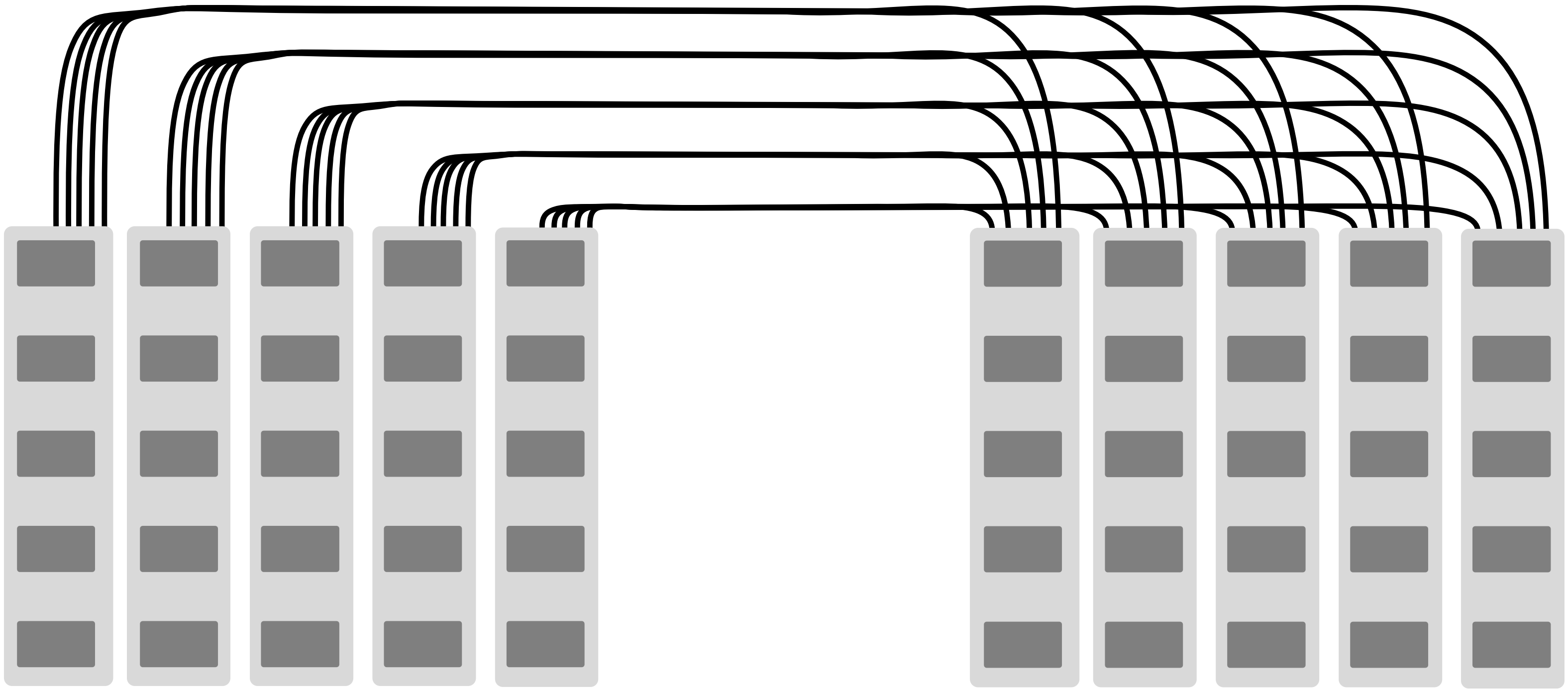
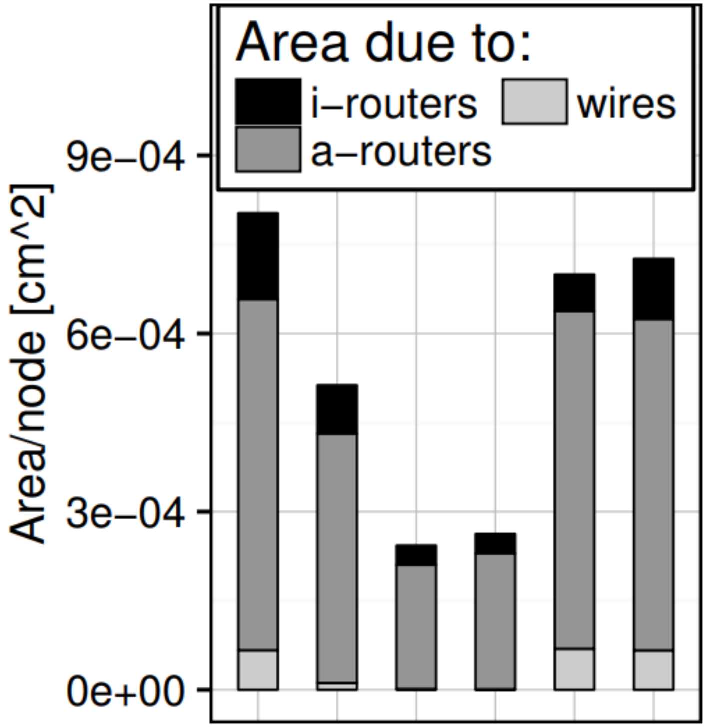
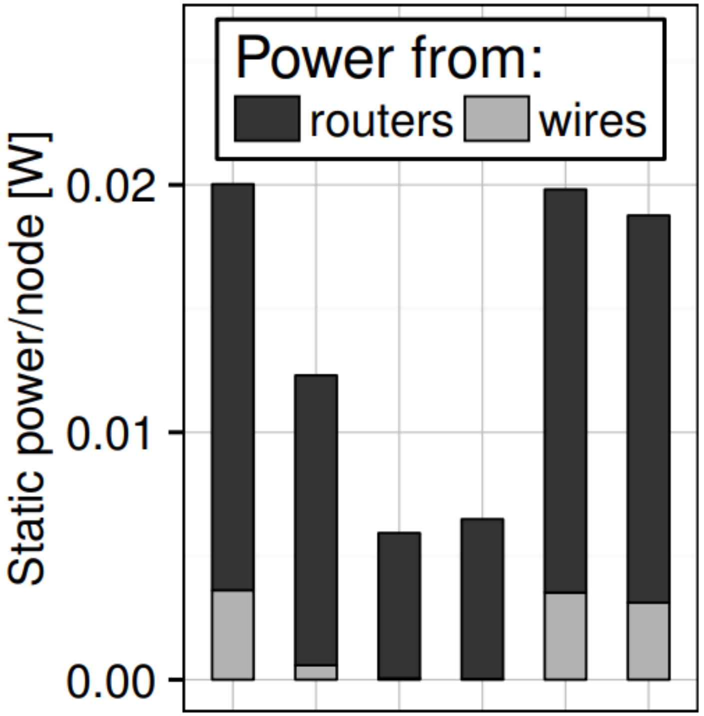


Groups form a fully-connected bipartite graph

Slim Fly on Chip – First Attempt
So how does it Fare?





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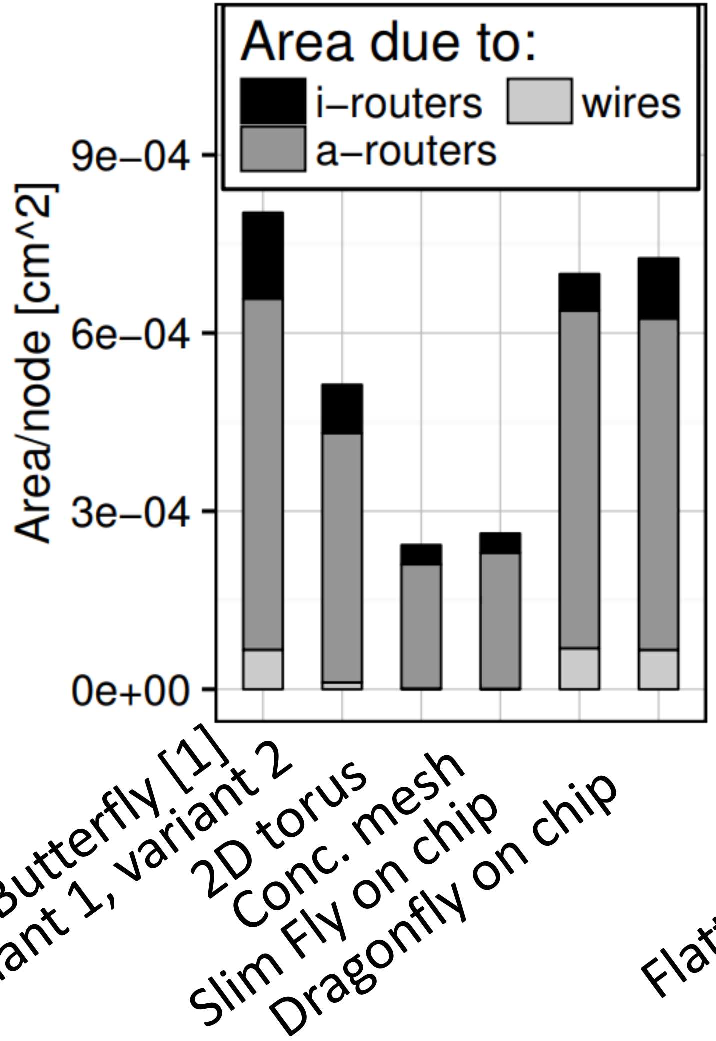

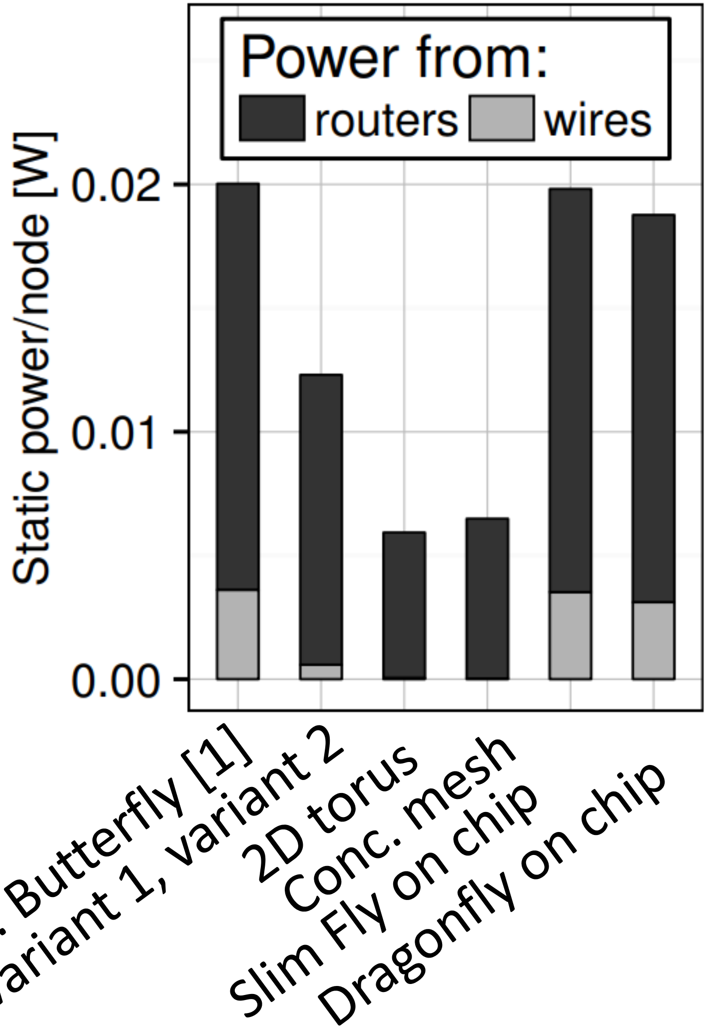

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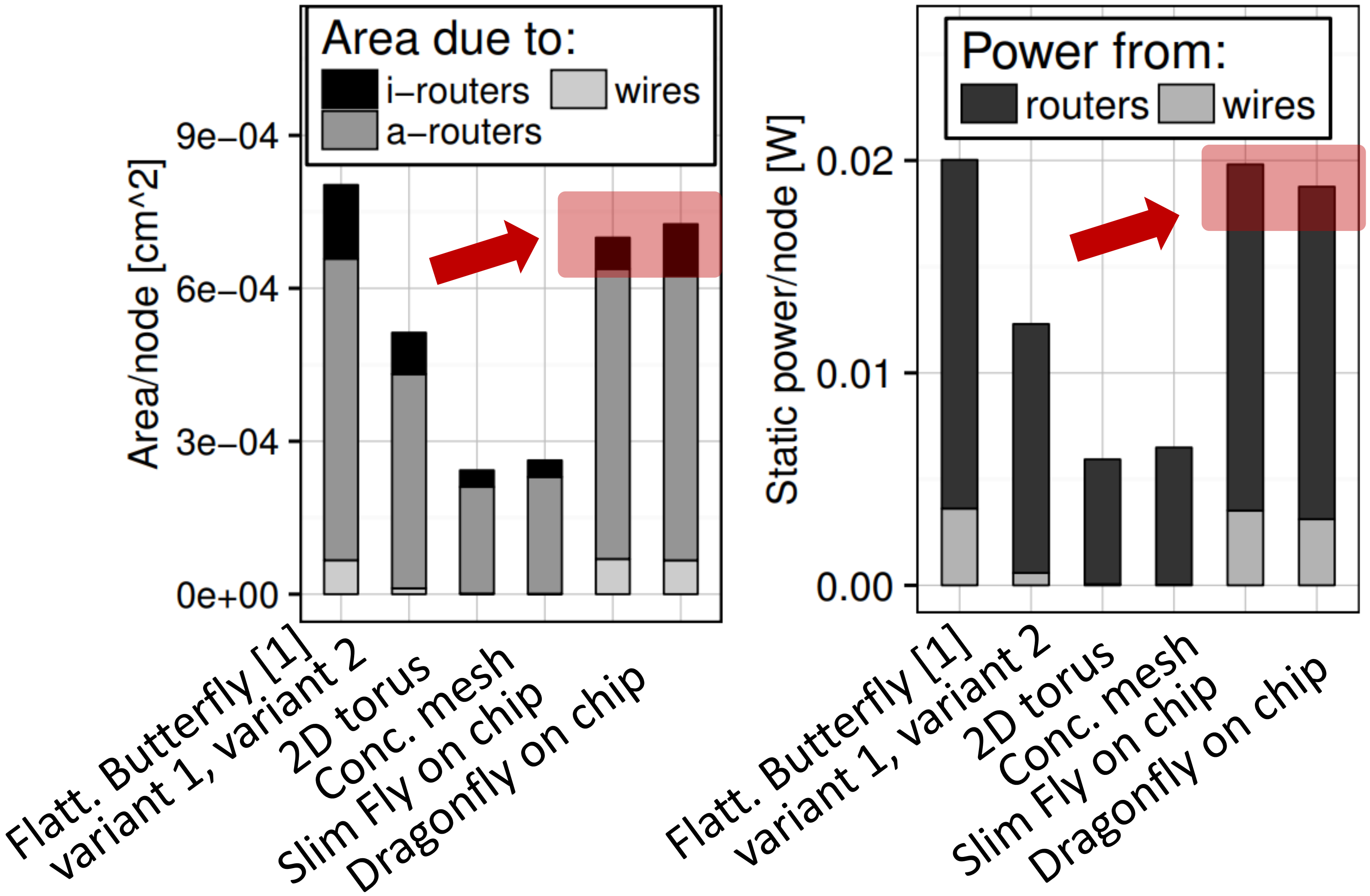

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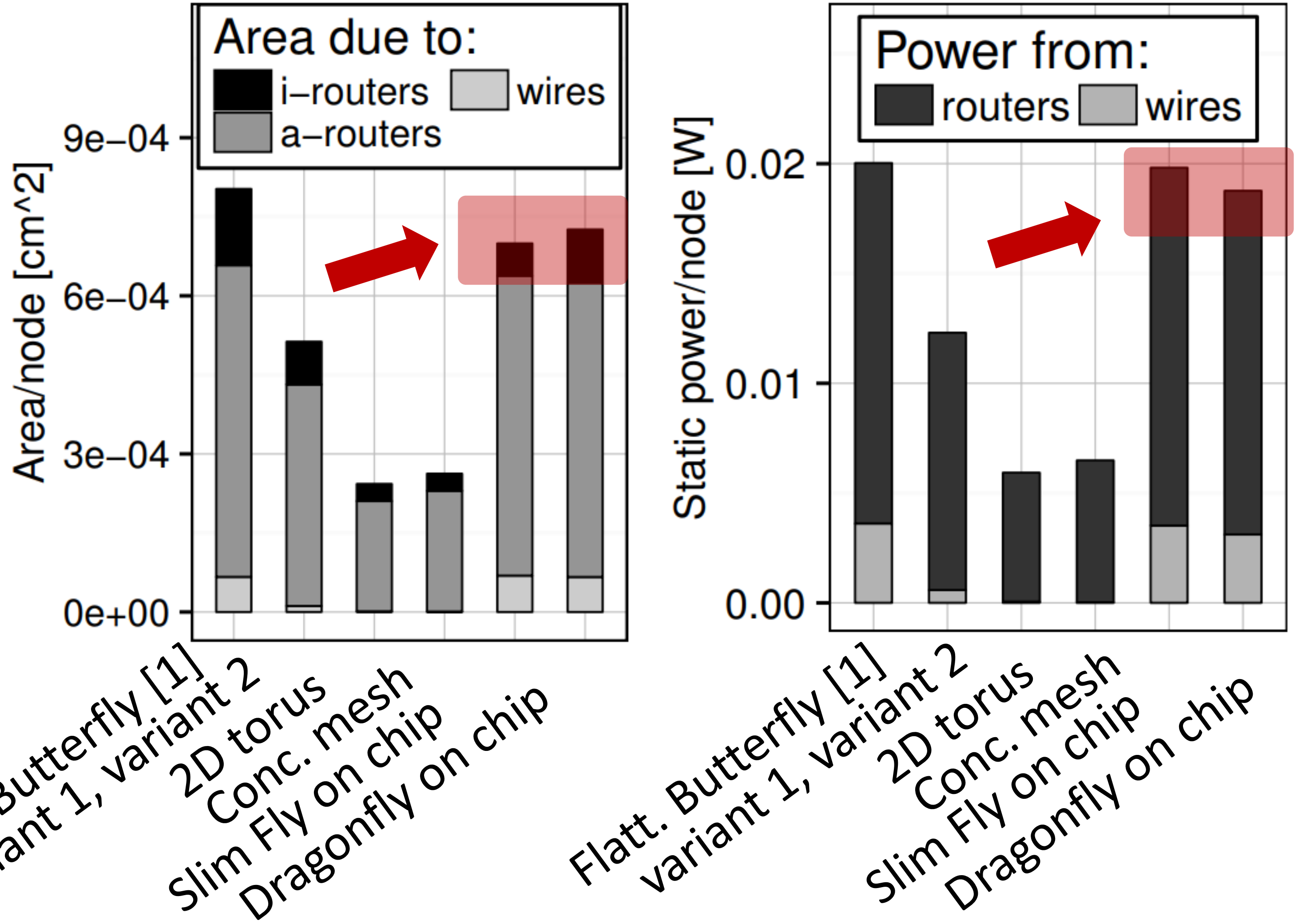

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Why?

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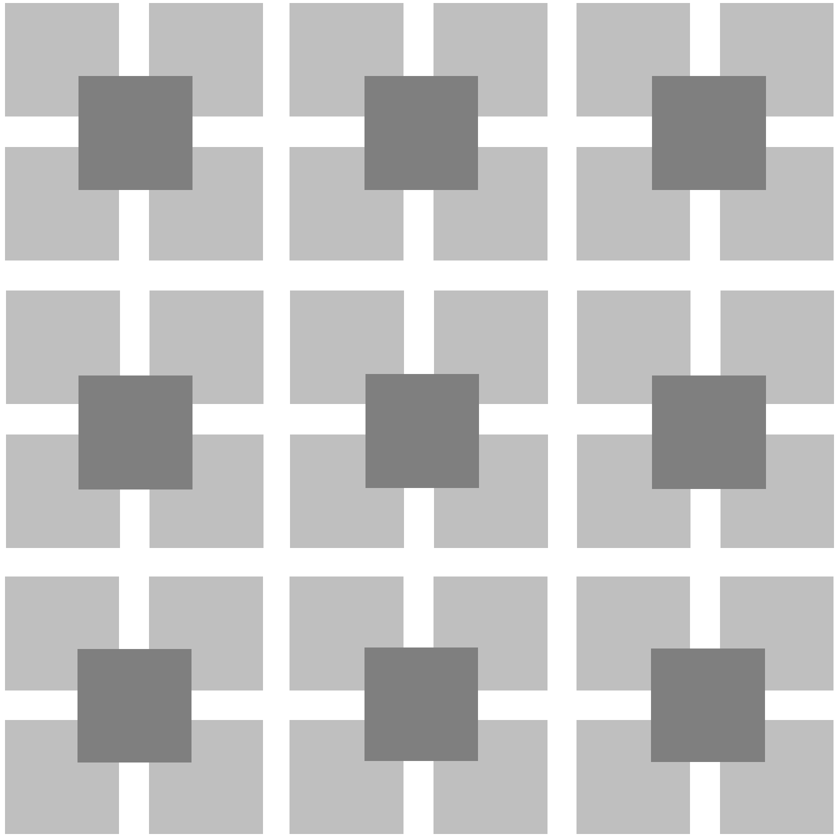
What are the problems with the simple on-chip Slim Fly?

Problems with Simple On-Chip Slim Fly, Part 1

Near-best radix-size-diameter tradeoff, but...



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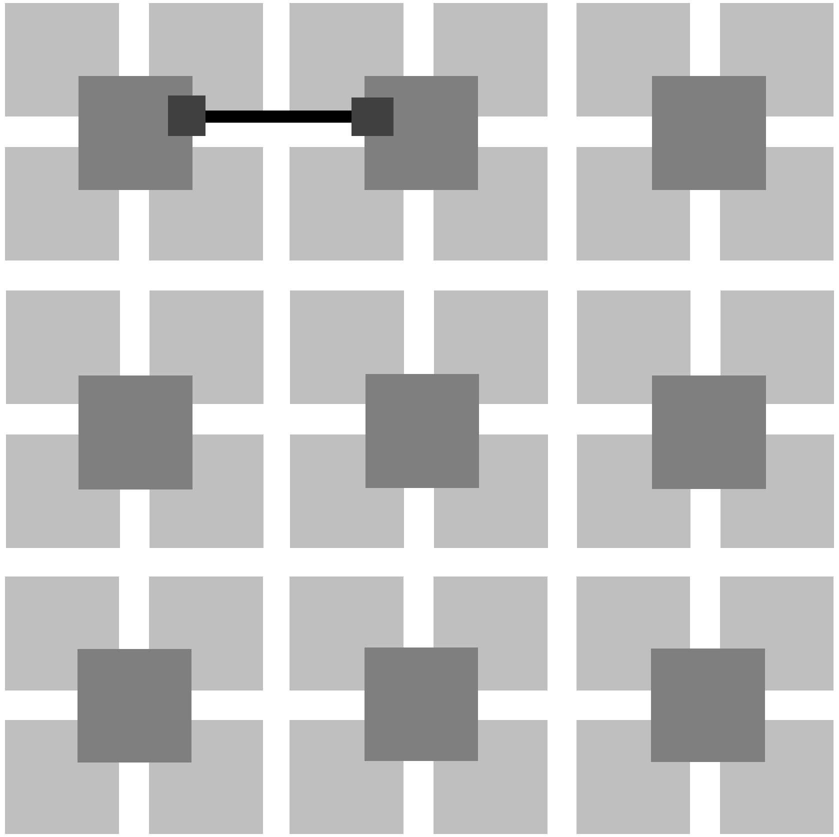

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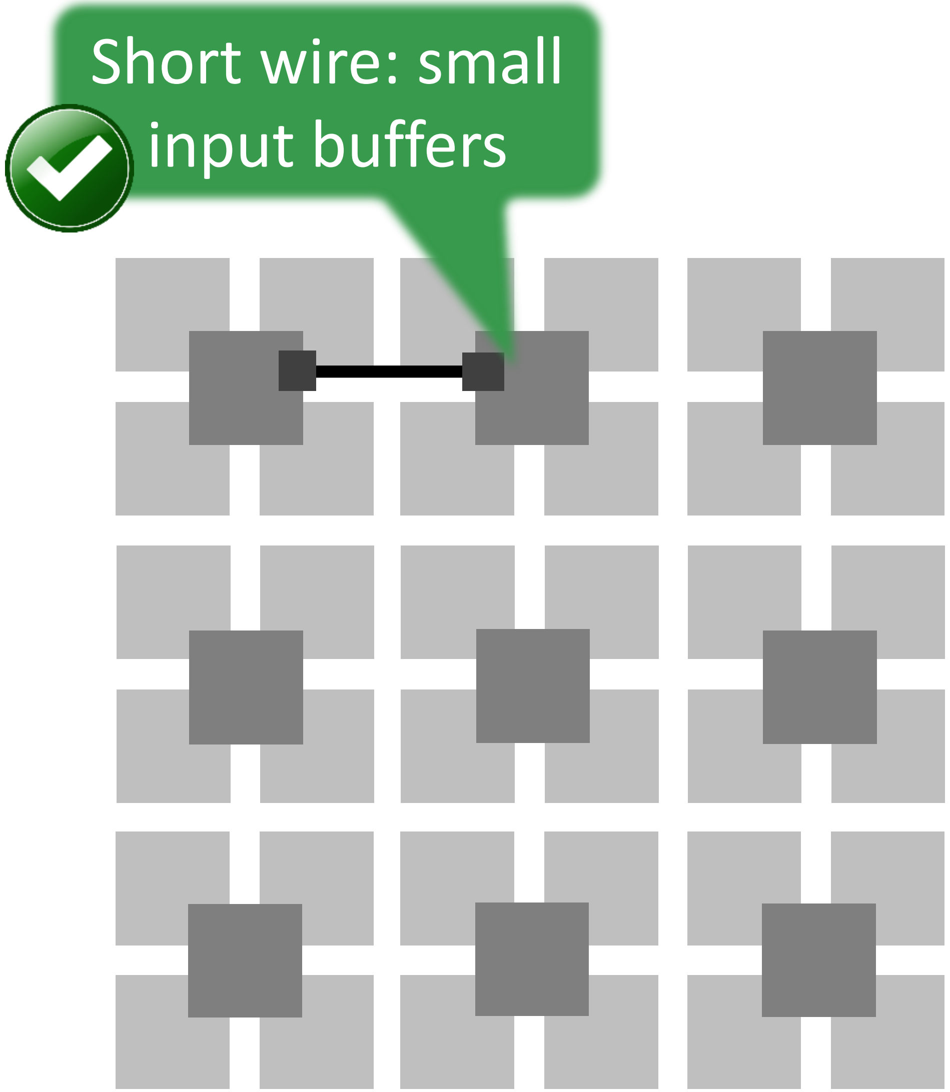

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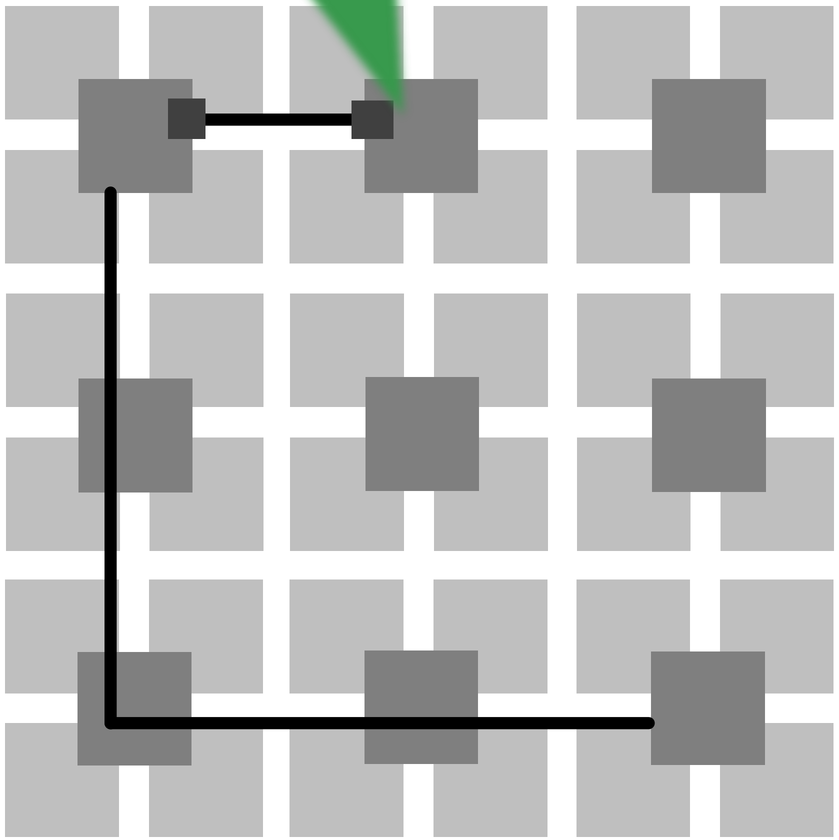
Near-best radix-size-diameter tradeoff, but...

Short wire: small input buffers



PROBLEMS WITH SIMPLE ON-CHIP SLIM FLY, PART 1

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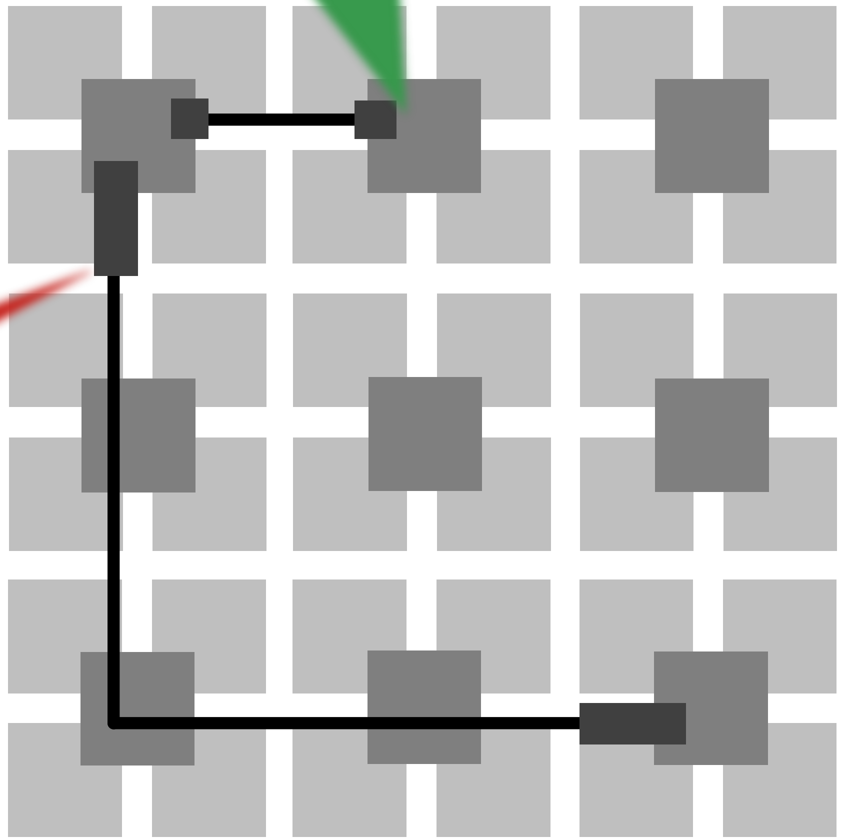

Problems with Simple On-Chip Slim Fly, Part 2

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Network radix k'	Concentration p	$p/\left\lceil \frac{k'}{2} \right\rceil$ **	Network size N	Router count N_r	Input param. q
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Problems with Simple On-Chip Slim Fly, Part 2

Various Slim Fly configurations

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There are few Slim Flies that satisfy various on-chip technological constraints

How to solve these problems?

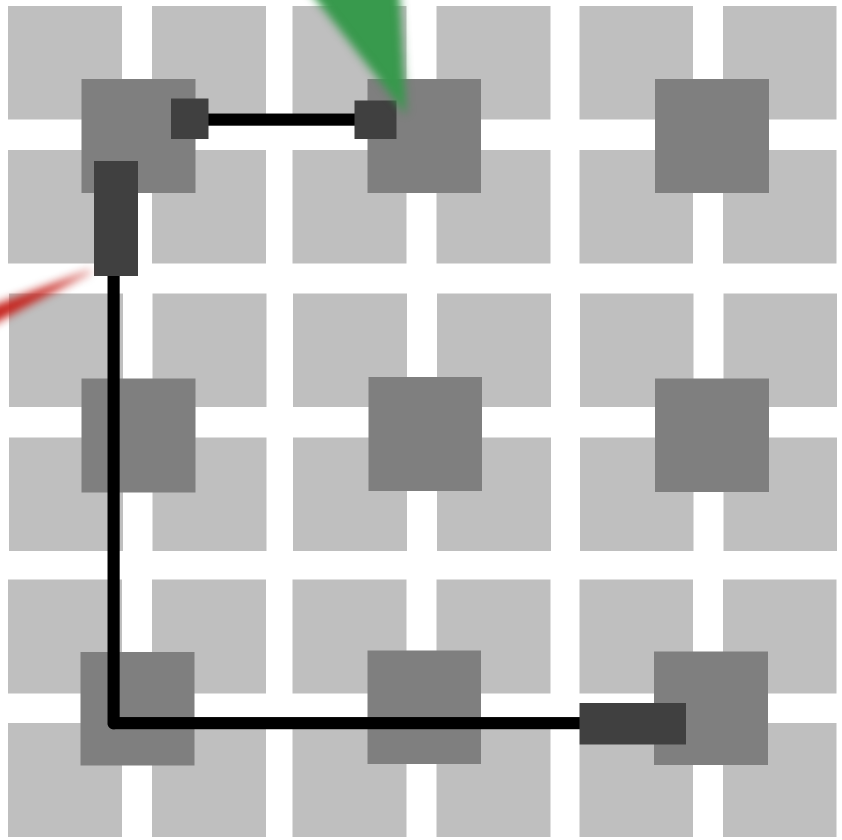
Solution: Slim NoC Part I

New cost and area models, new layouts

Near-best radix-size-diameter tradeoff, but...

Short wire: small input buffers

Long wire: traversing the whole die requires large input buffers for full link utilization



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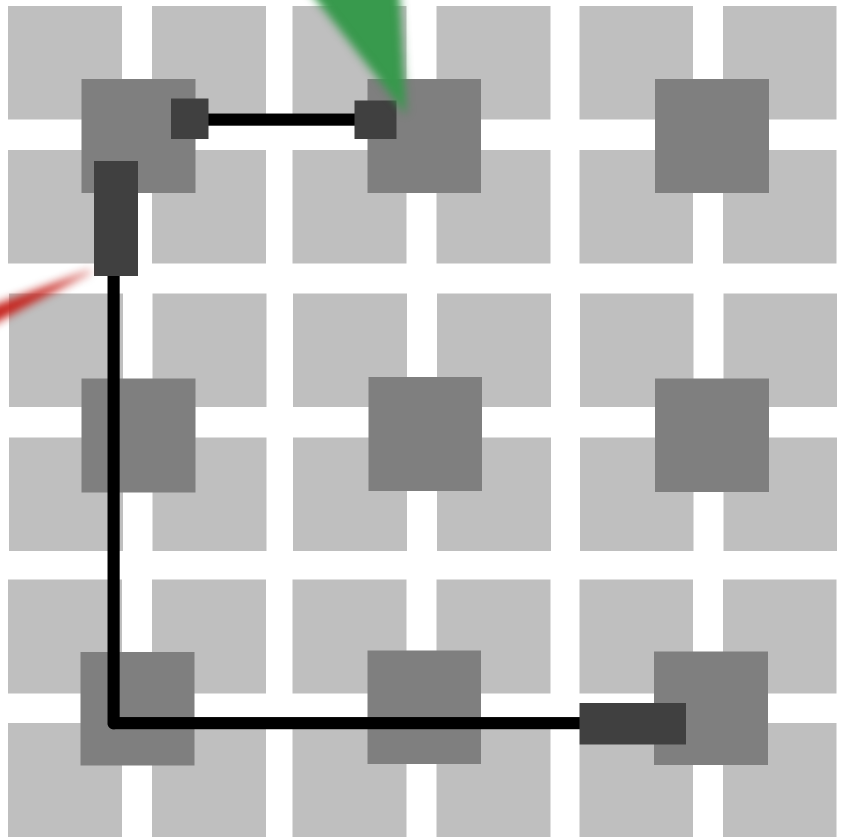

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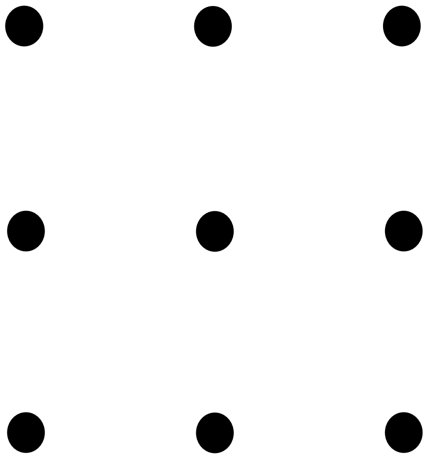

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NEW COST AND AREA MODELS, NEW LAYOUTS

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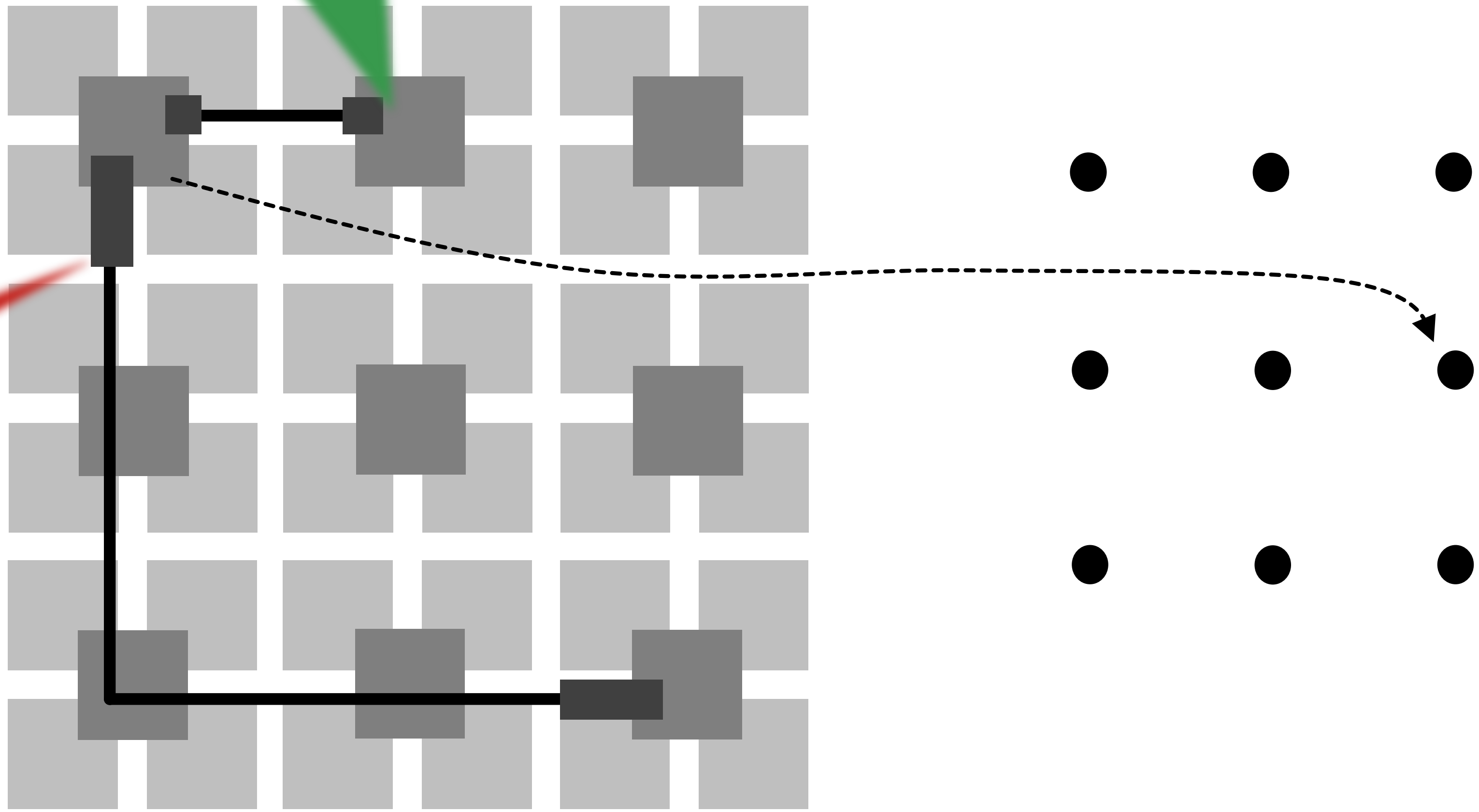

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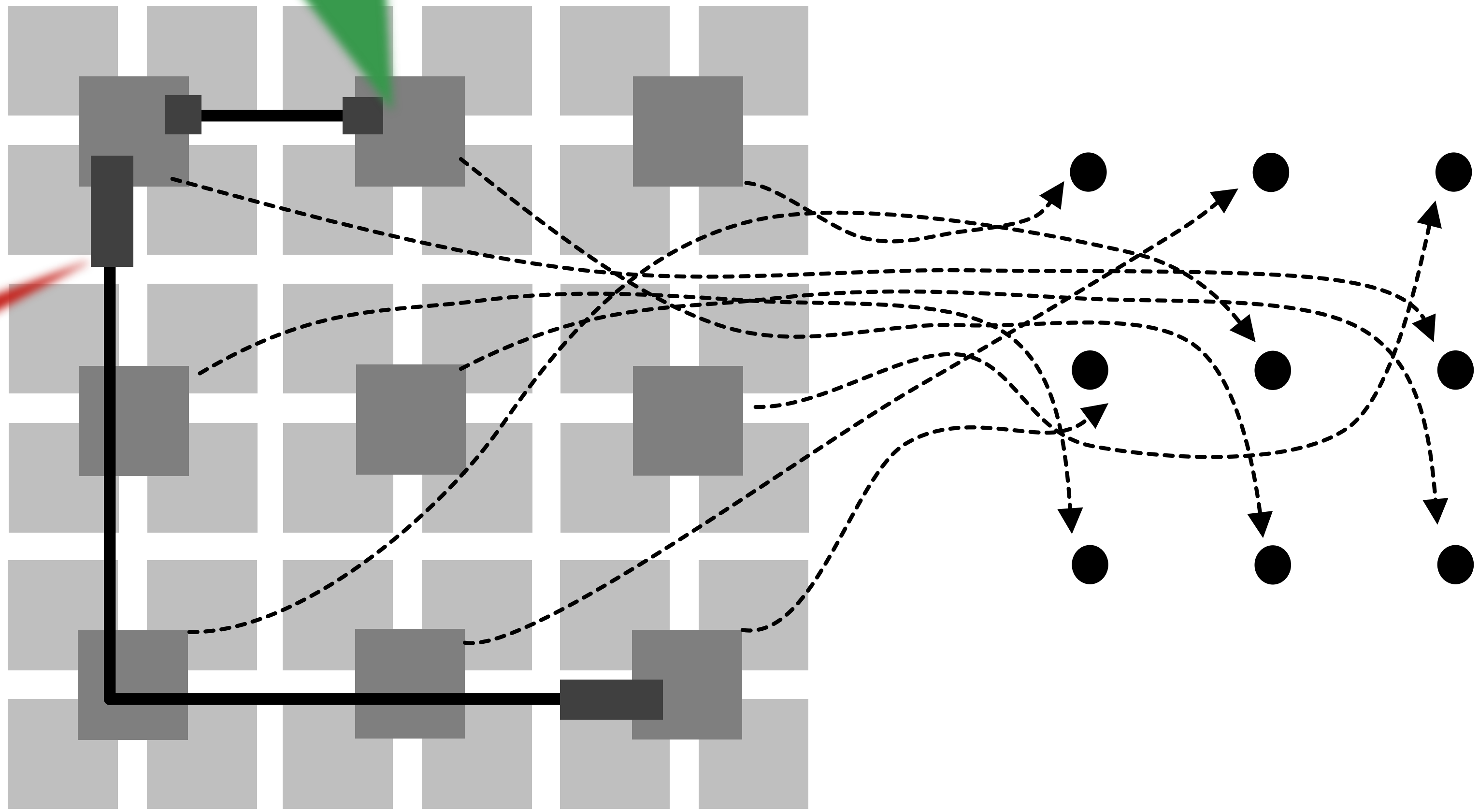

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The model must be generic to allow for arbitrary layouts.

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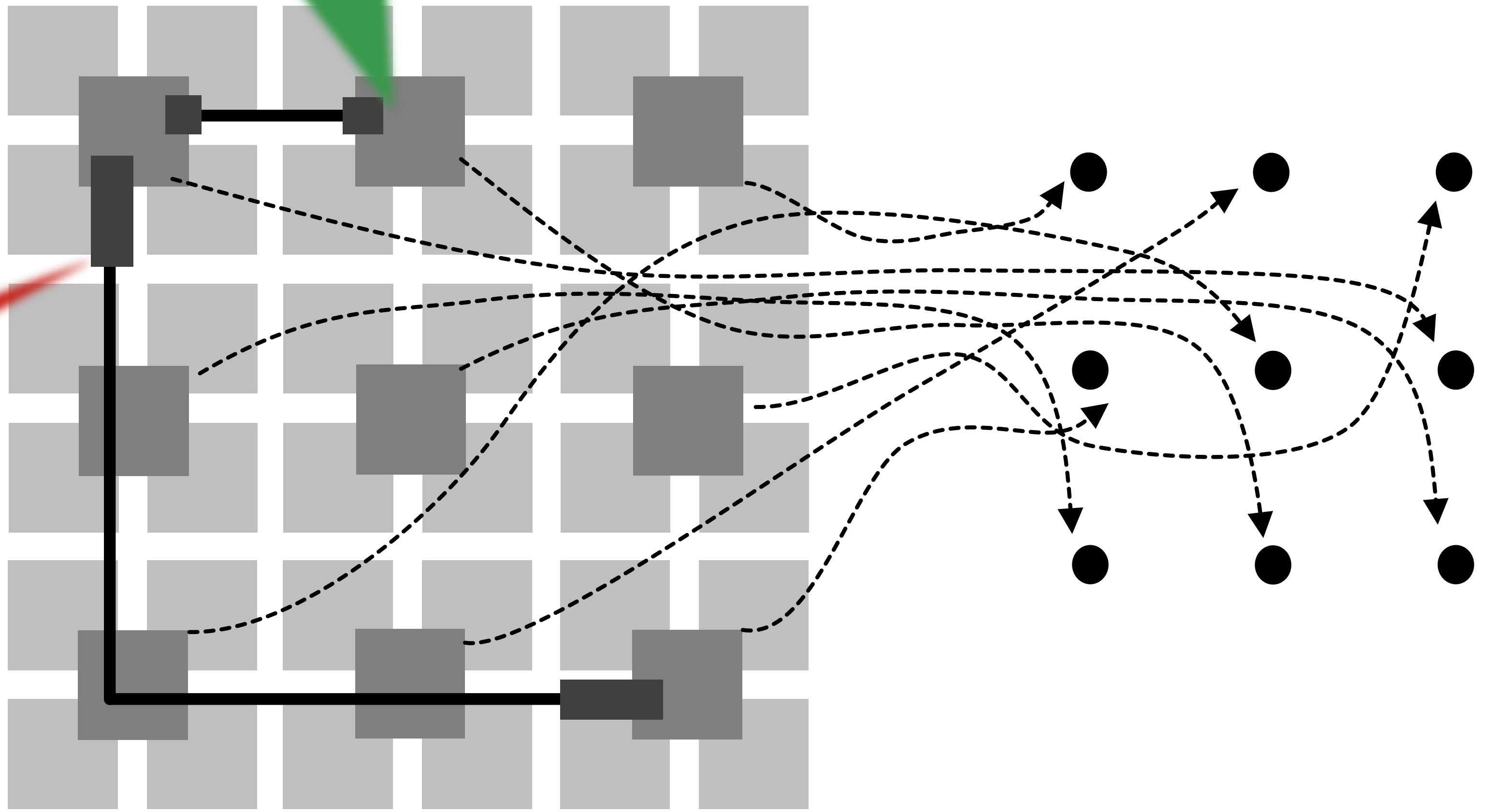

Solution: Slim NoC Part I

New cost and area models, new layouts

Near-best radix-size-diameter tradeoff, but...

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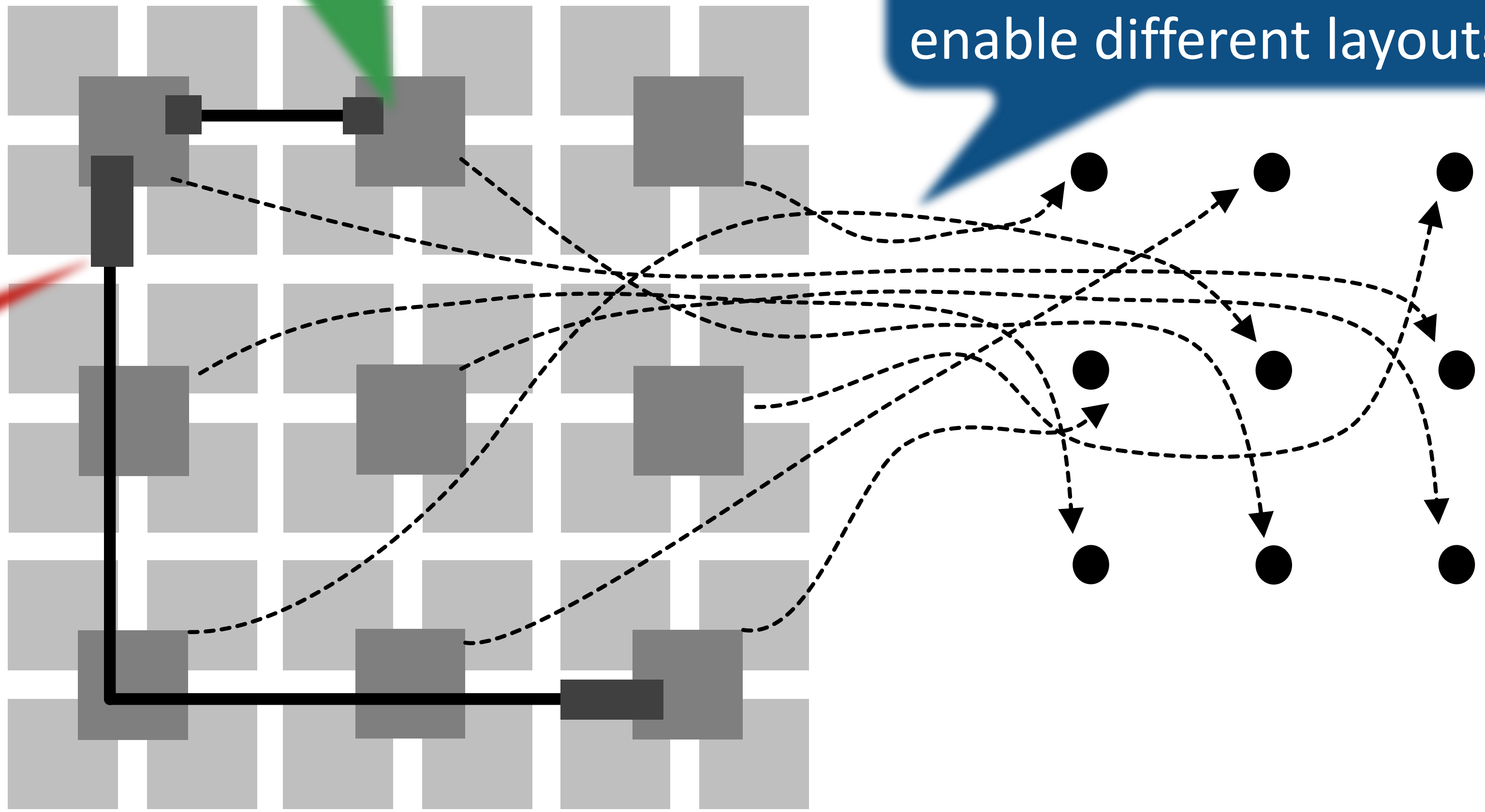
Short wire: small input buffers

The model must be generic to allow for arbitrary layouts.

Different mappings ("sets of arrows") enable different layouts



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NEW COST AND AREA MODELS, NEW LAYOUTS

How to select a mapping?

SOLUTION: SLIM NOC Part I

NEW COST AND AREA MODELS, NEW LAYOUTS

How to select a mapping?

Minimize the average wire length (*M*) :

$$M = \frac{\text{Sum of distances}}{\text{Number of links}}$$

Solution: Slim NoC Part I

New cost and area models, new layouts

How to select a mapping?

Minimize the average wire length (*M*) :

$$M = \frac{\text{Sum of distances}}{\text{Number of links}}$$

Minimize the total buffer area (*Δ*):

$$\Delta = \sum_{\text{All router pairs } i, j} \text{If } i, j \text{ are connected, } (\varepsilon_{ij} = 1) \text{ add the size of a buffer from } i \text{ to } j$$

Solution: Slim NoC Part I

New cost and area models, new layouts

How to select a mapping?

ILP formulation: many more details for reproducibility and genericness, check the paper ☺

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$$\Phi(i,j) = 1 \text{ if } |x_i - x_j| > |y_i - y_j|, \text{ and 0 otherwise}$$

$$\Psi(i,j) = 1 \text{ if } |x_i - x_j| \leq |y_i - y_j|, \text{ and 0 otherwise.}$$

$$\phi_{ij}(k,l) = \begin{cases} 1, & \text{if } k = x_i \wedge \min\{y_i, y_j\} \leq l \leq \max\{y_i, y_j\} \\ 1, & \text{if } l = y_j \wedge \min\{x_i, x_j\} \leq k \leq \max\{x_i, x_j\} \\ 0, & \text{otherwise} \end{cases}$$

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$$\sum_{i=1}^{N_r} \sum_{j=1}^{N_r} \varepsilon_{ij}[\phi_{ij}(k,l)\Phi(i,j) + \psi_{ij}(k,l)\Psi(i,j)] \leq W$$

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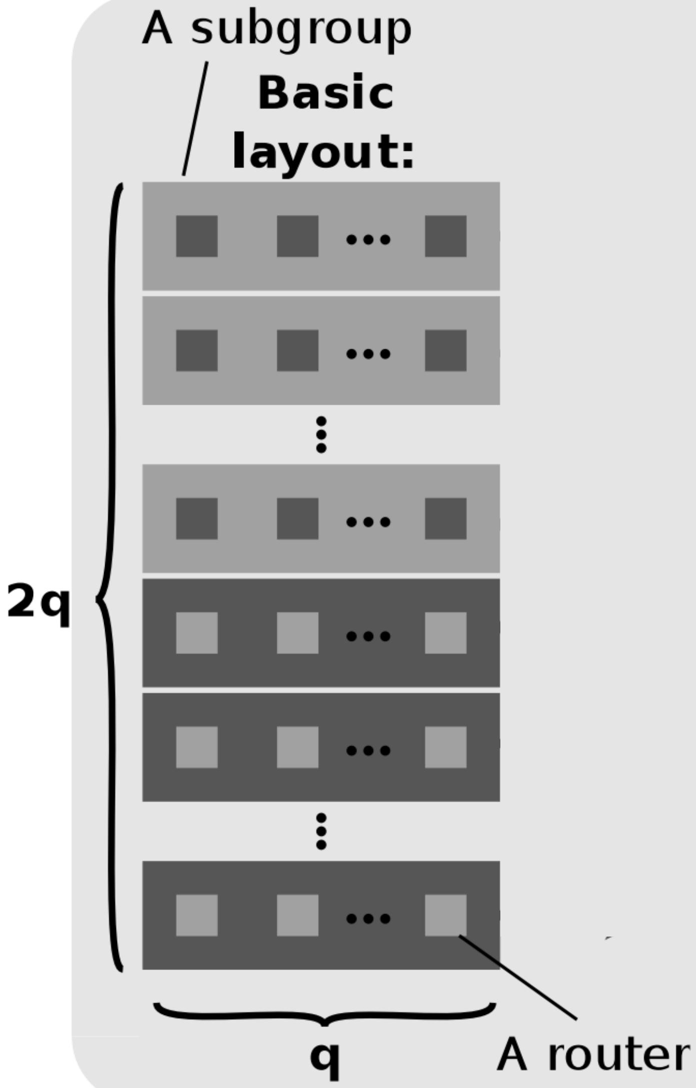
New cost and area models, new layouts

Let us see some layouts



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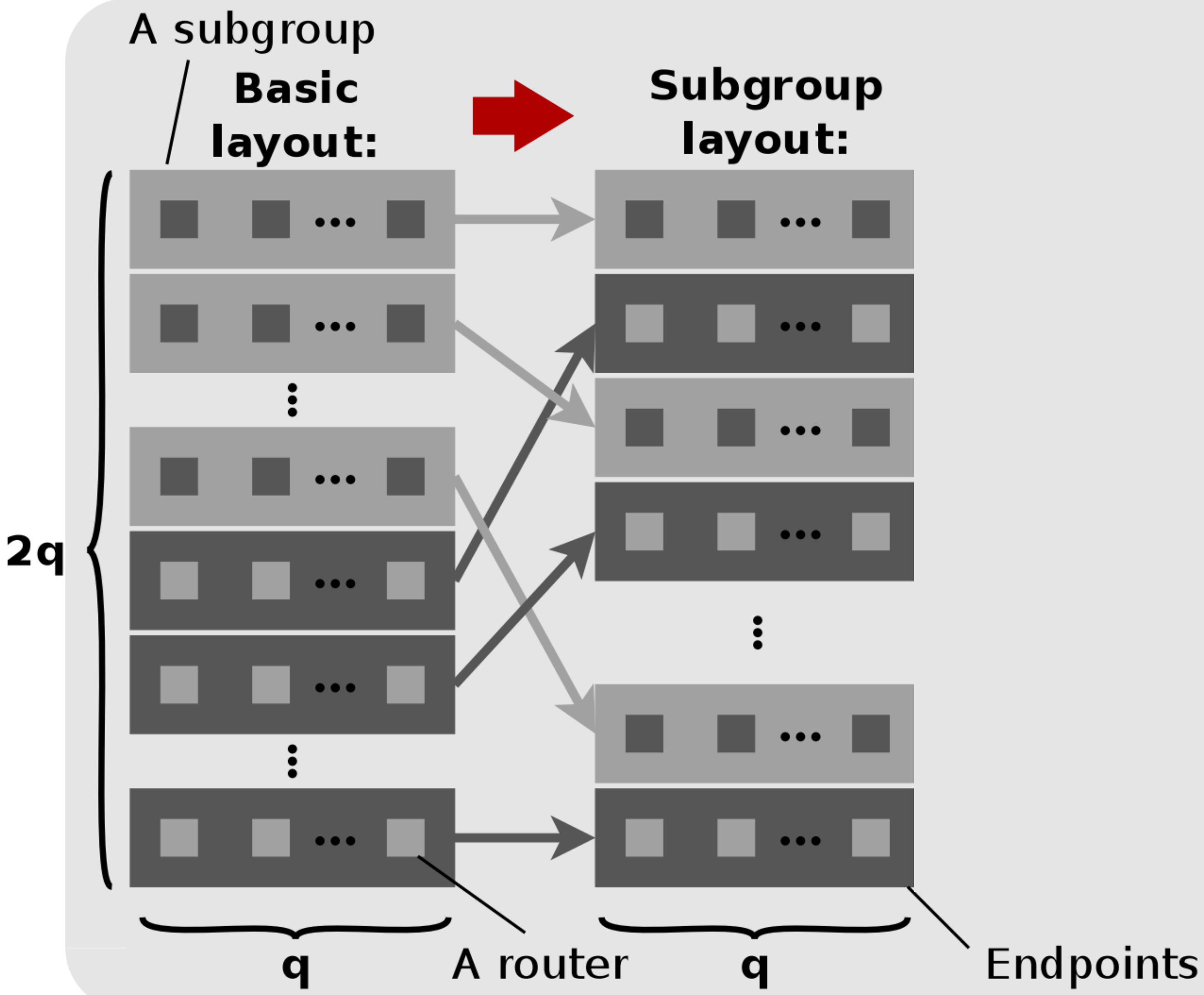

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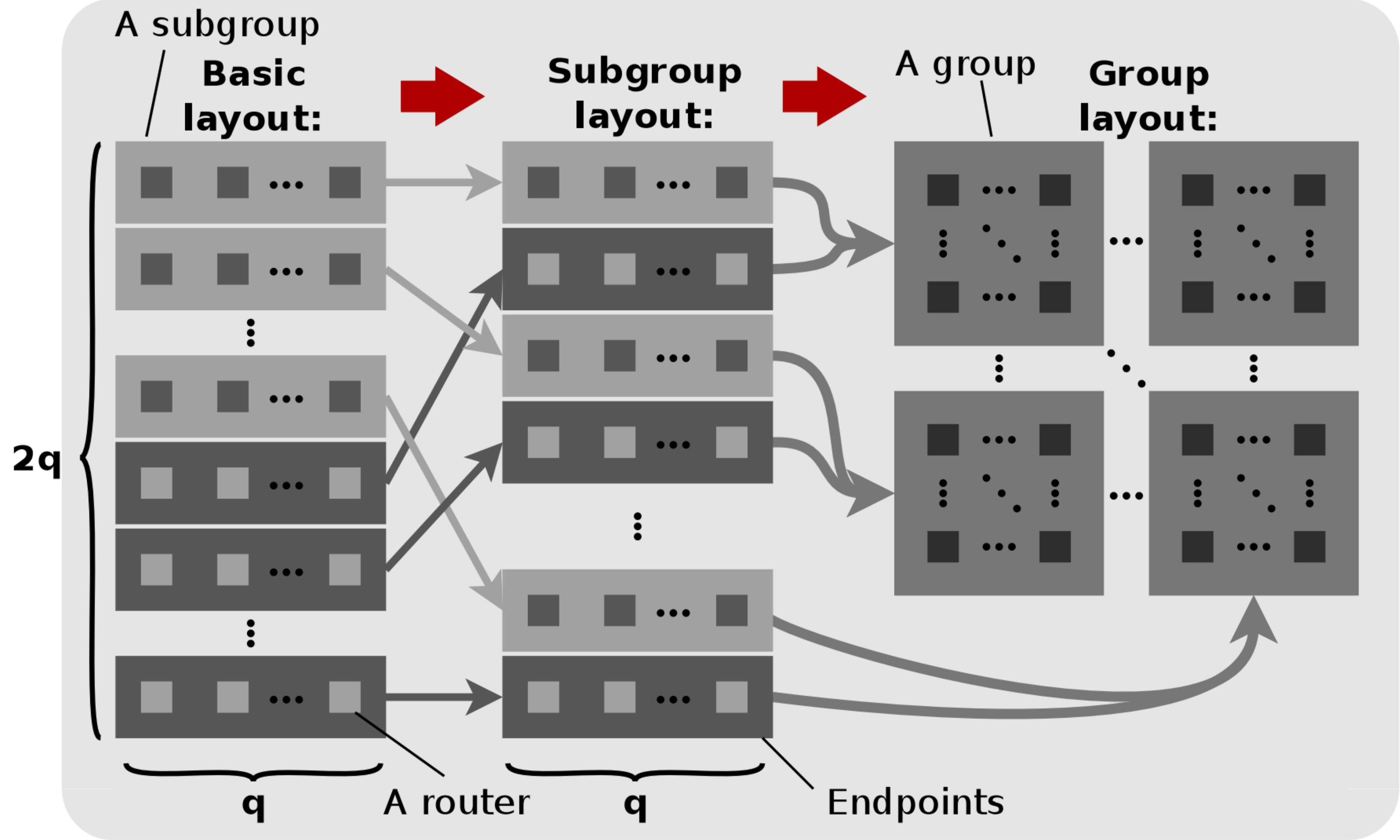

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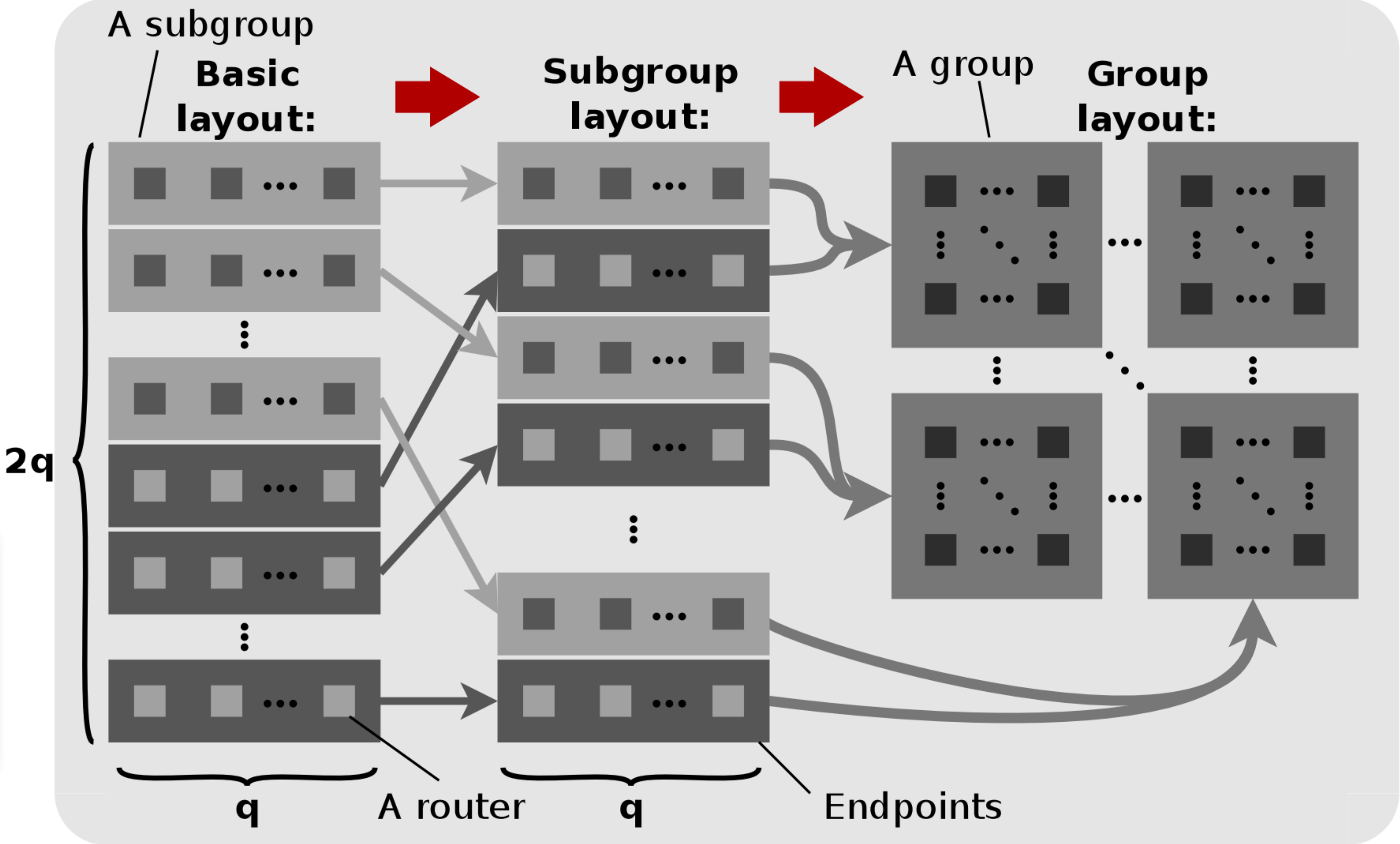
What difference do they make for lengths of wires?



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Let us see some layouts

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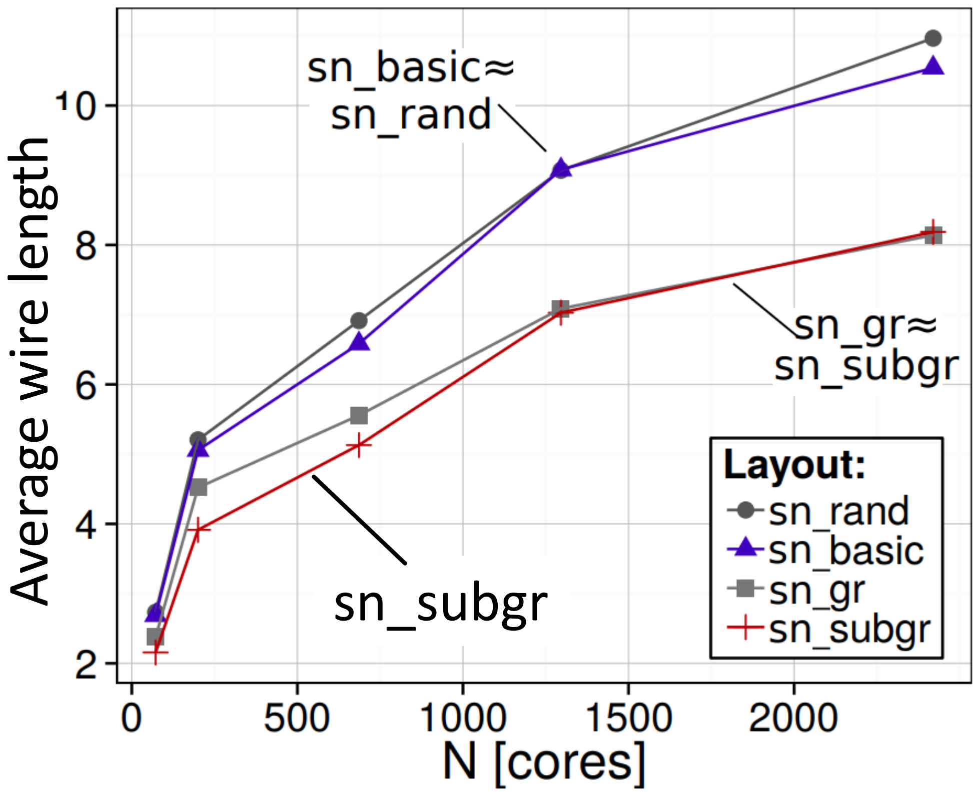
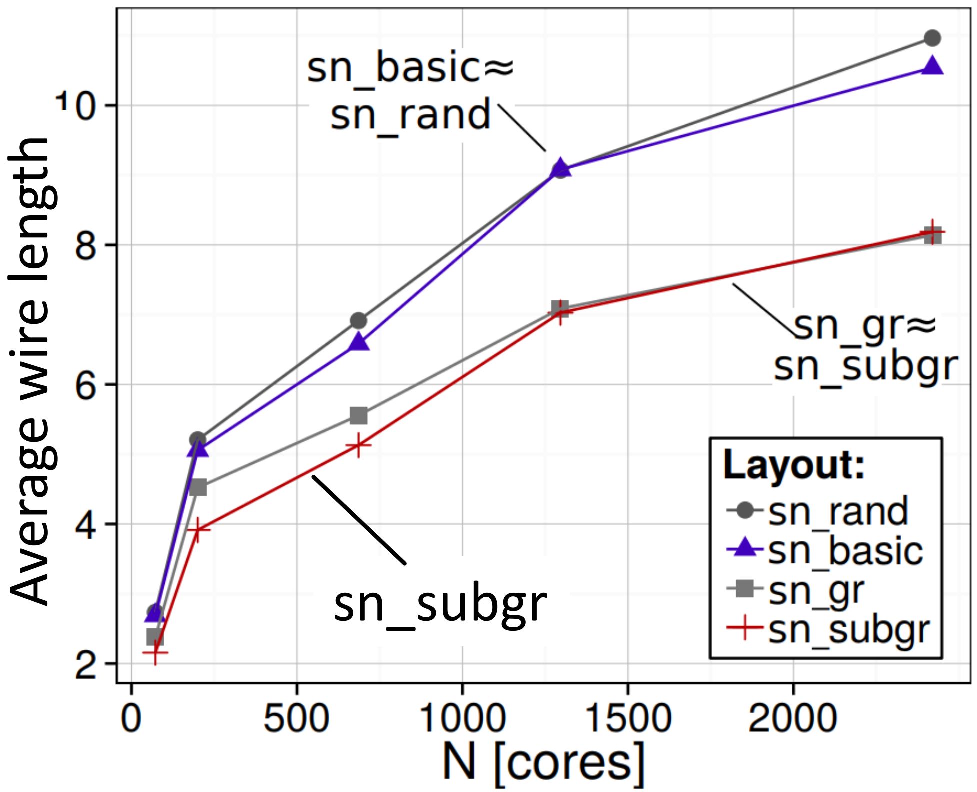


SOLUTION: SLIM NOC Part I

NEW COST AND AREA MODELS, NEW LAYOUTS

Let us see some layouts



What difference do they make for lengths of wires?

The "subgroup layout" (sn_subgr) is best for 200 nodes
The "group layout" (sn_gr) is best for 1296 nodes
(it reduces wiring complexity)

Now let's move to the second problem...

Solution: Slim NoC Non-Prime Finite Fields

Part II

Are there configurations with...

...number of nodes/routers being a power of two?

...equally many cores on each die side?

...equally many routers on each die side?

...equally many router groups on each die side?

Various Slim Fly configurations

Network radix k'	Concentration p	$p/\lceil \frac{k'}{2} \rceil$ **	Network size N	Router count N_r	Input param. q
3	2	100%	16	8	2
5	2	66%	36	18	3
5	3	100%	54	18	3
5	4	133%	72	18	3
7	3	75%	150	50	5
7	4	100%	200	50	5
7	5	120%	250	50	5
11	4	66%	392	98	7
11	5	83%	490	98	7
11	6	100%	588	98	7
11	7	116%	686	98	7
11	8	133%	784	98	7

There are few Slim Flies that satisfy various on-chip technological constraints

No need to pay attention to all these numbers ☺

Solution: Slim NoC Non-Prime Finite Fields

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12	4	66%	**512**	128	8
12	5	83%	640	128	8
12	6	100%	768	128	8
12	7	116%	896	128	8
12	8	133%	**1024**	128	8
13	5	71%	810	162	9
13	6	85%	972	162	9
13	7	100%	1134	162	9
13	8	114%	1296	162	9

Solution: Slim NoC Non-Prime Finite Fields

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SOLUTION: SLIM NOC — NON-PRIME FINITE FIELDS

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Are there configurations with...

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Solution: Slim NoC Part II
Non-Prime Finite Fields

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How to develop such a finite field?

Solution: Slim NoC
Non-Prime Finite Fields

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Solution: Slim NoC
Non-Prime Finite Fields

How to develop such a finite field?

Recap: a finite field $\mathcal{F}_q$

Assuming q is **prime**:

$\mathcal{F}_q = \mathbb{Z}/q\mathbb{Z}$

$= \{0,1, \ldots, q-1\}$

(with modular arithmetic).

Example: $q = 5$

50 routers

$\mathcal{F}_5 = \{0,1,2,3,4\}$

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...with instruction tables that define operations on the field.

How to develop such a finite field?

Example: $q = 9$

162 routers

$\mathcal{F}_9 = \{0,1,2,u,v,w,x,y,z\}$

+	0	1	2	u	v	w	x	y	z
0	0	1	2	u	v	w	x	y	z
1	1	2	0	v	w	u	y	z	x
2	2	0	1	w	u	v	z	x	y
u	u	v	w	x	y	z	0	1	2
v	v	w	u	y	z	x	1	2	0
w	w	u	v	z	x	y	2	0	1
x	x	y	z	0	1	2	u	v	w
y	y	z	x	1	2	0	v	w	u
z	z	x	y	2	0	1	w	u	v

Addition

×	0	1	2	u	v	w	x	y	z
0	0	0	0	0	0	0	0	0	0
1	0	1	2	u	v	w	x	y	z
2	0	2	1	x	z	y	u	w	v
u	0	u	x	2	w	z	1	v	y
v	0	v	z	w	x	1	y	2	u
w	0	w	y	z	1	u	v	x	2
x	0	x	u	1	y	v	2	z	w
y	0	y	w	v	2	x	z	u	1
z	0	z	v	y	u	2	w	1	x

Multiplication

elem	$-$*elem*
0	0
1	2
2	0
u	x
v	z
w	y
x	u
y	w
z	v

Inverse

Solution: Slim NoC
Non-Prime Finite Fields

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v	v	w	u	y	z	x	1	2	0
w	w	u	v	z	x	y	2	0	1
x	x	y	z	0	1	2	u	v	w
y	y	z	x	1	2	0	v	w	u
z	z	x	y	2	0	1	w	u	v

Addition

u	0	u	x	2	w	z	1	v	y
v	0	v	z	w	x	1	y	2	u
w	0	w	y	z	1	u	v	x	2
x	0	x	u	1	y	v	2	z	w
y	0	y	w	v	2	x	z	u	1
z	0	z	v	y	u	2	w	1	x

Multiplication

u	x
v	z
w	y
x	u
y	w
z	v

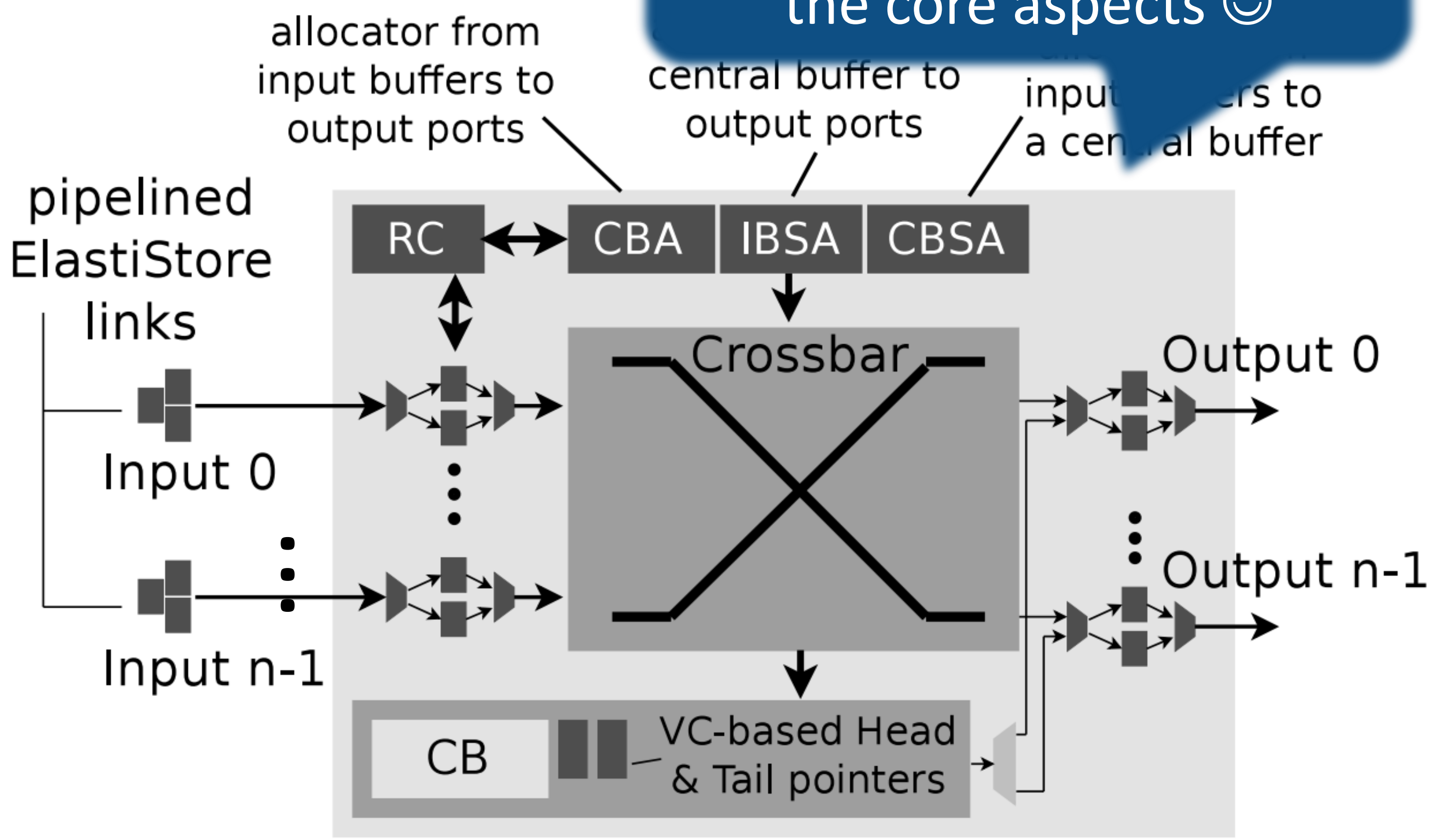
Inverse

Check the paper for details ☺

How do we optimize the router microarchitecture for Slim NoC to provide high performance and high efficiency?

Slim NoC Router Microarchitecture
Performance Optimizations Part III

Let's leave the details for the paper and just focus on the core aspects ☺



SLIM NOC ROUTER MICROARCHITECTURE
PERFORMANCE OPTIMIZATIONS Part III

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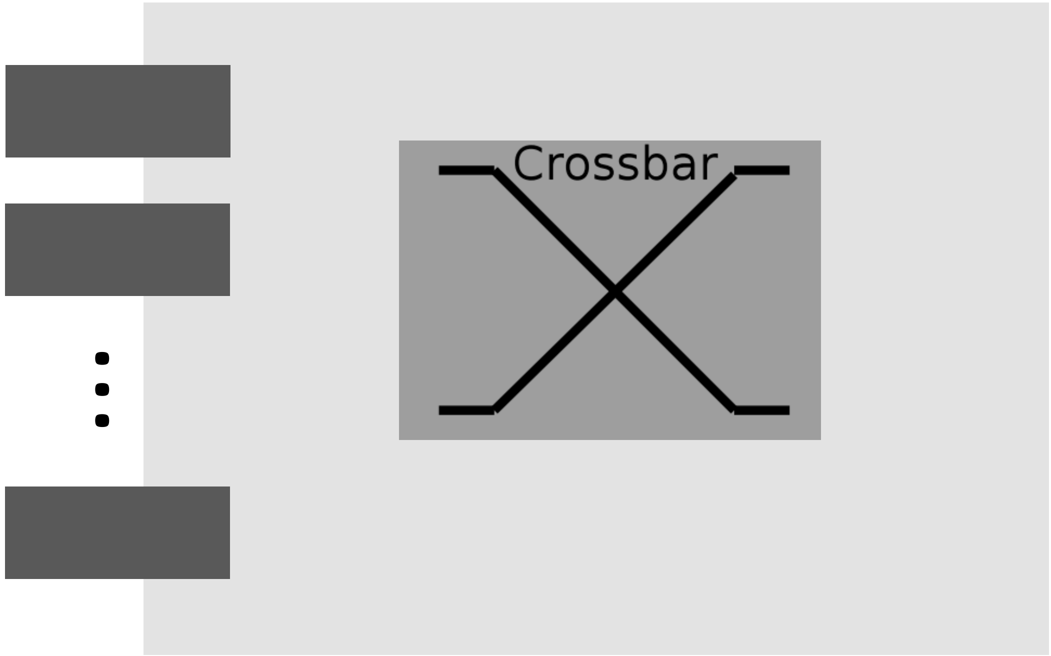

Slim NoC Router Microarchitecture
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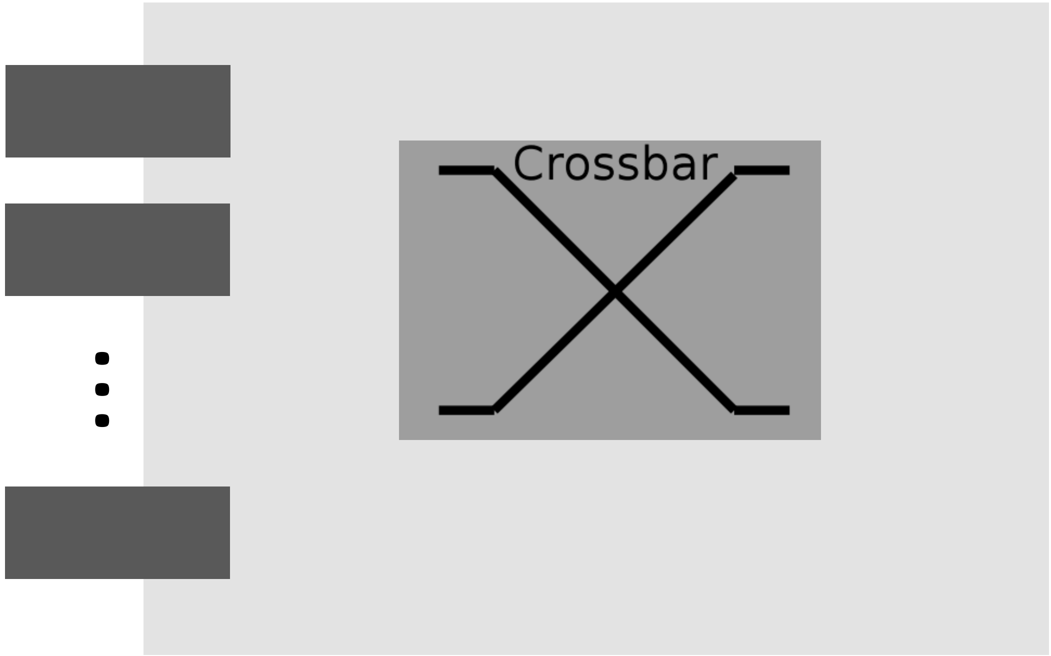

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Enhancement 1:
Elastic Buffer links [1]
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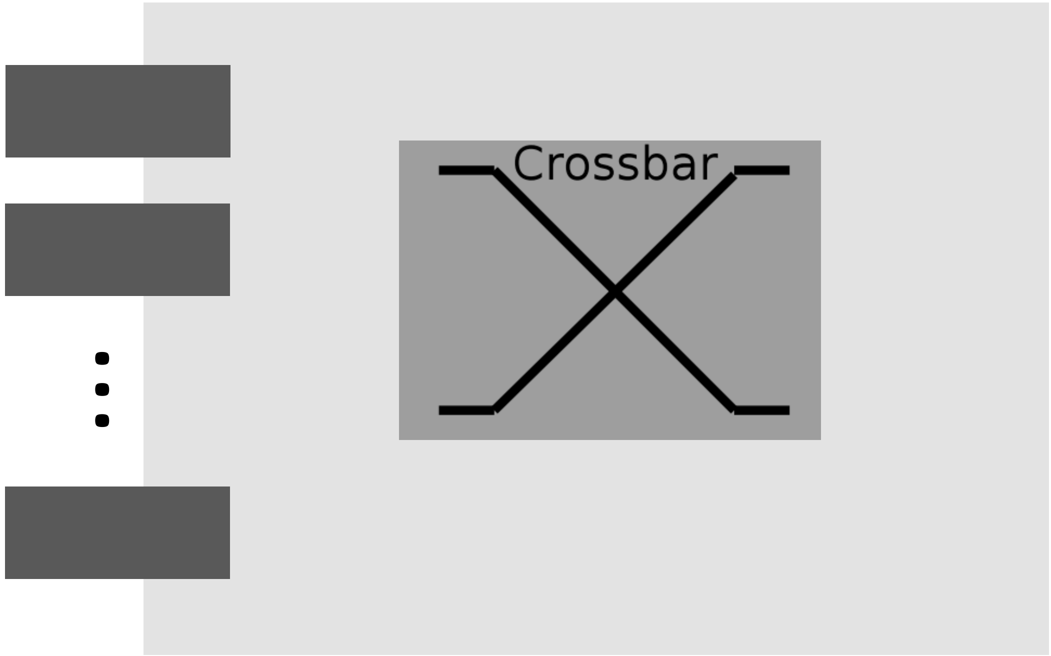

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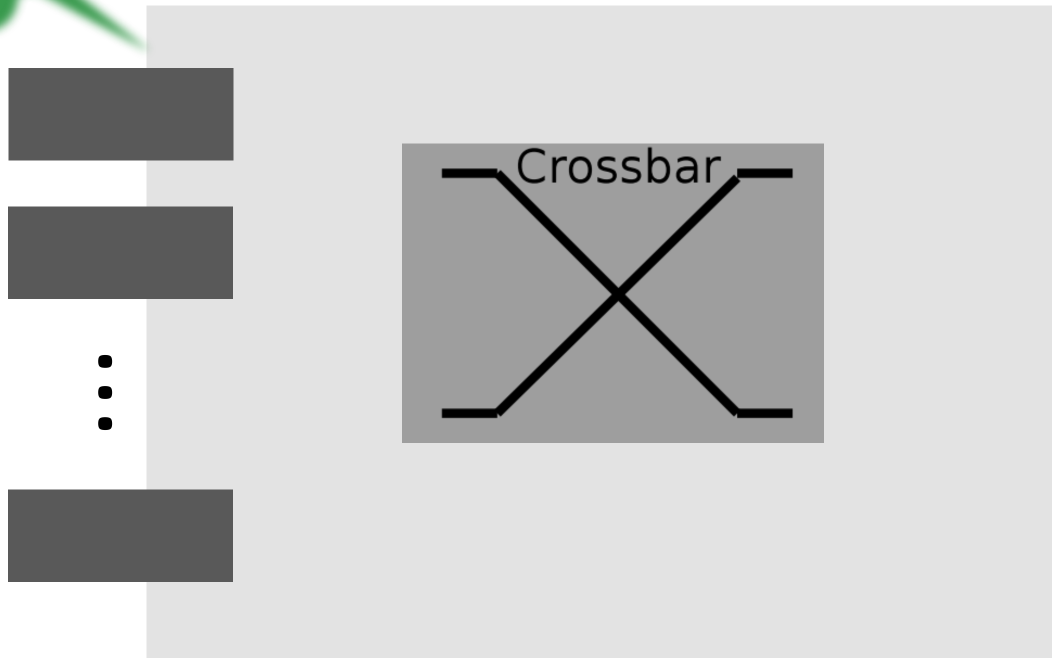
Provide deadlock-freedom



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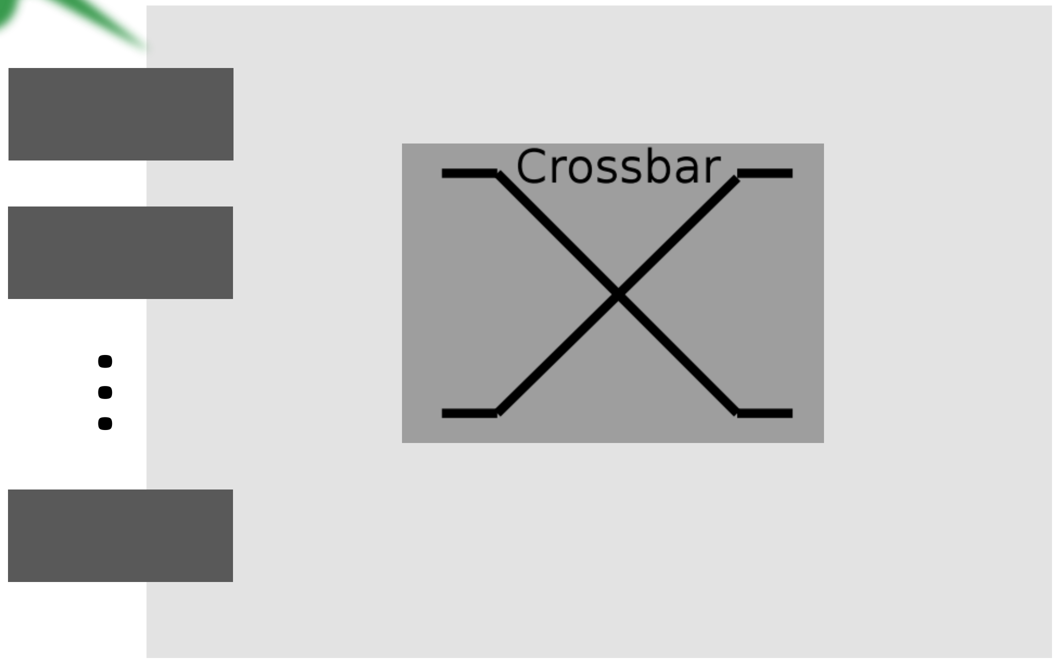
Provide deadlock-freedom

Enhancement 2:
SMART Links [3]

Drive links asynchronously and use repeaters for single-cycle wires



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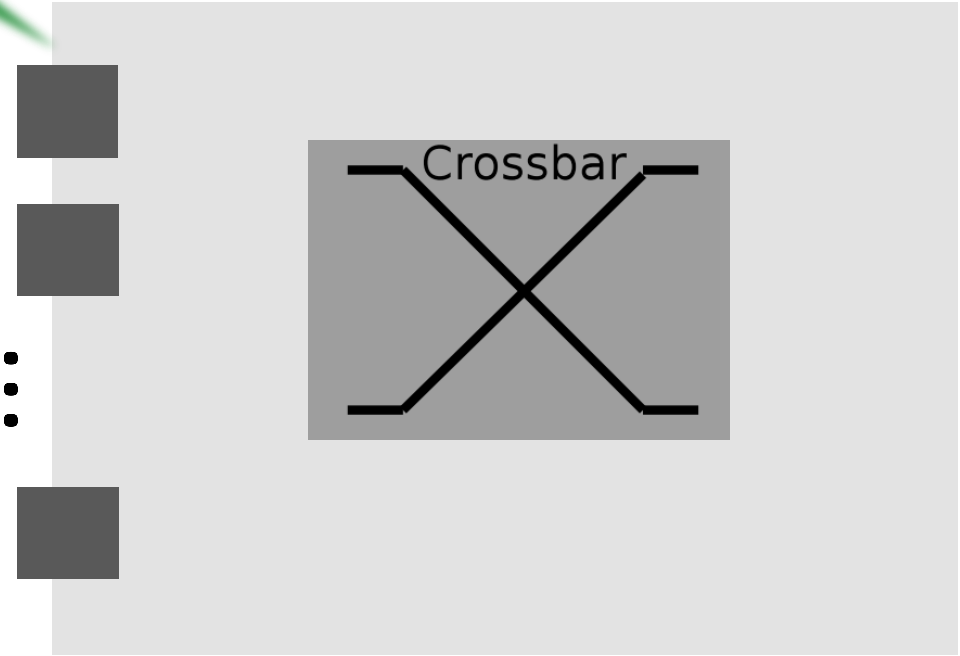

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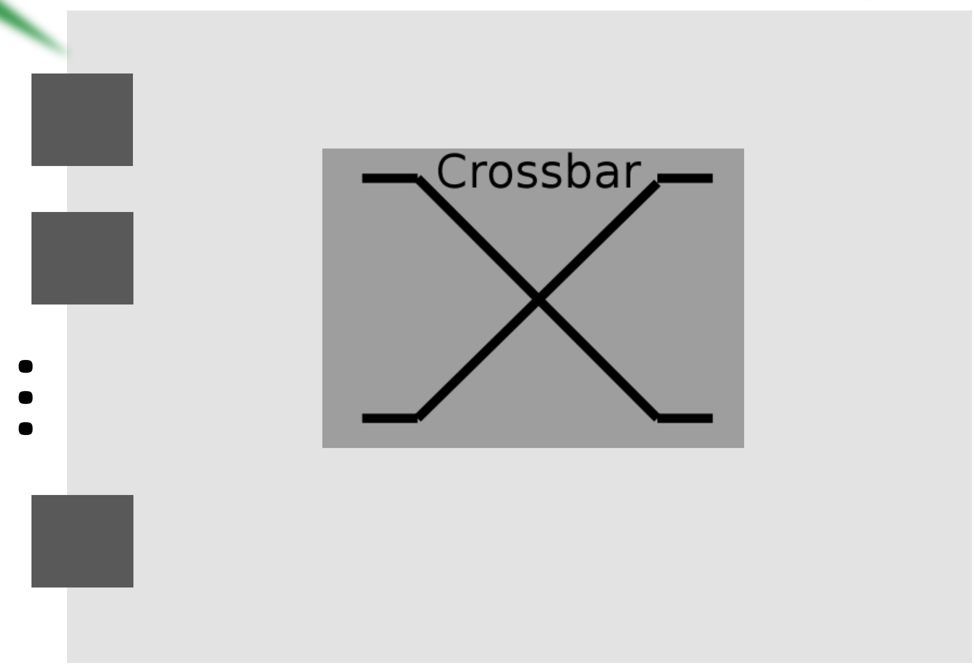
Enhancement 3: Central Buffers [4]



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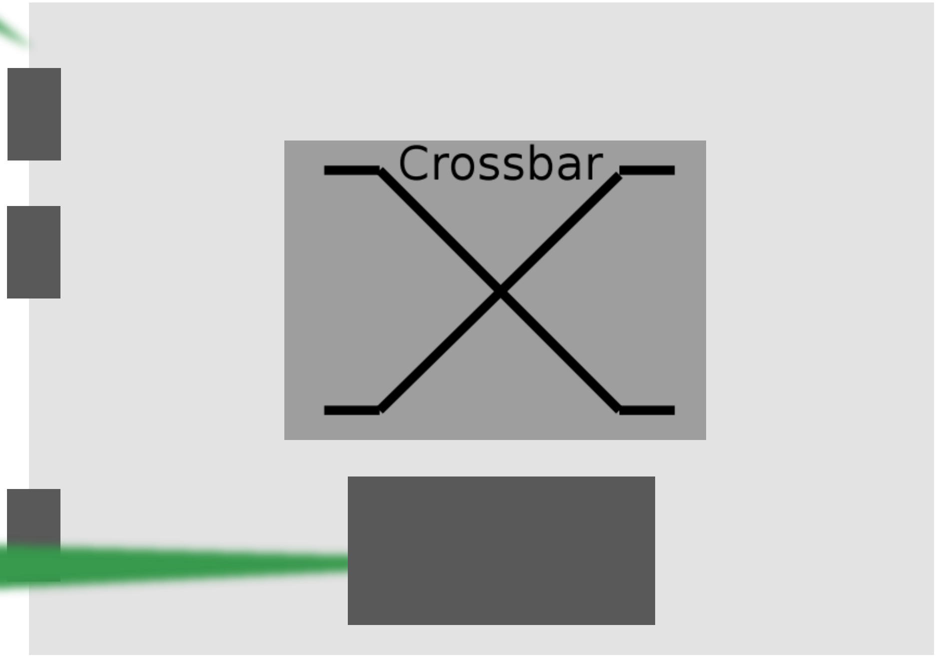
Enhancement 3:
Central Buffers [4]

Replace multi-flit input buffers with single-flit stating input buffers and add a central buffer



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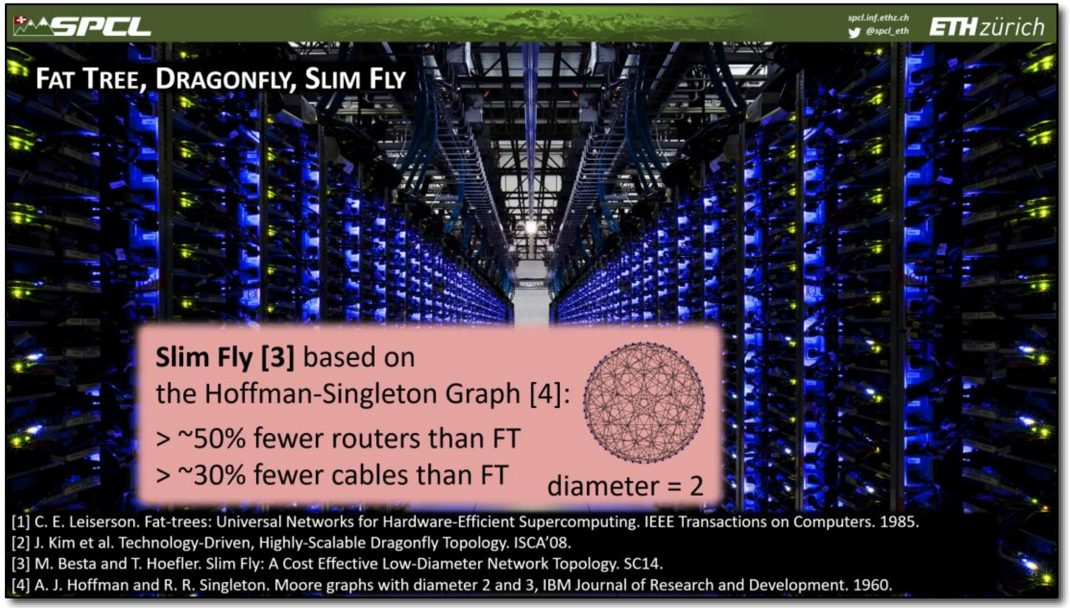

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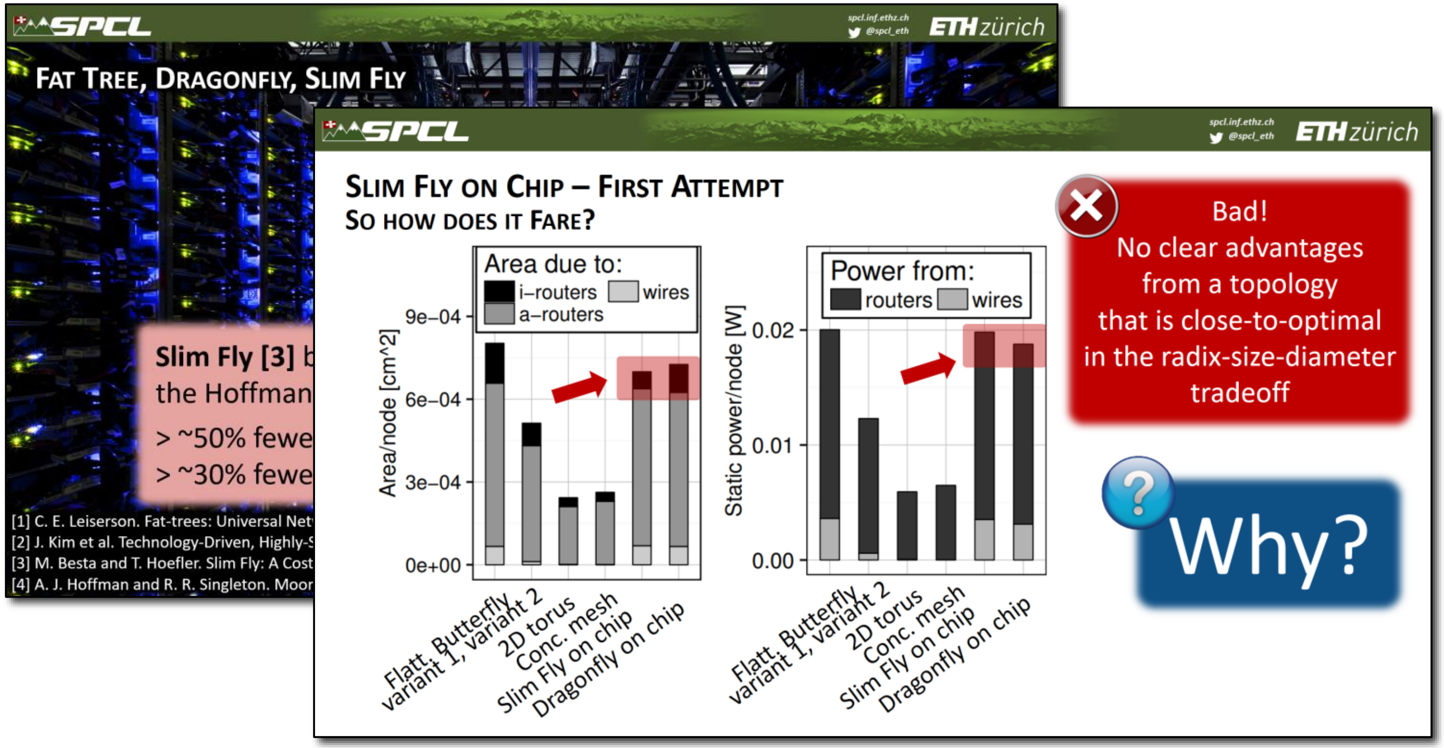

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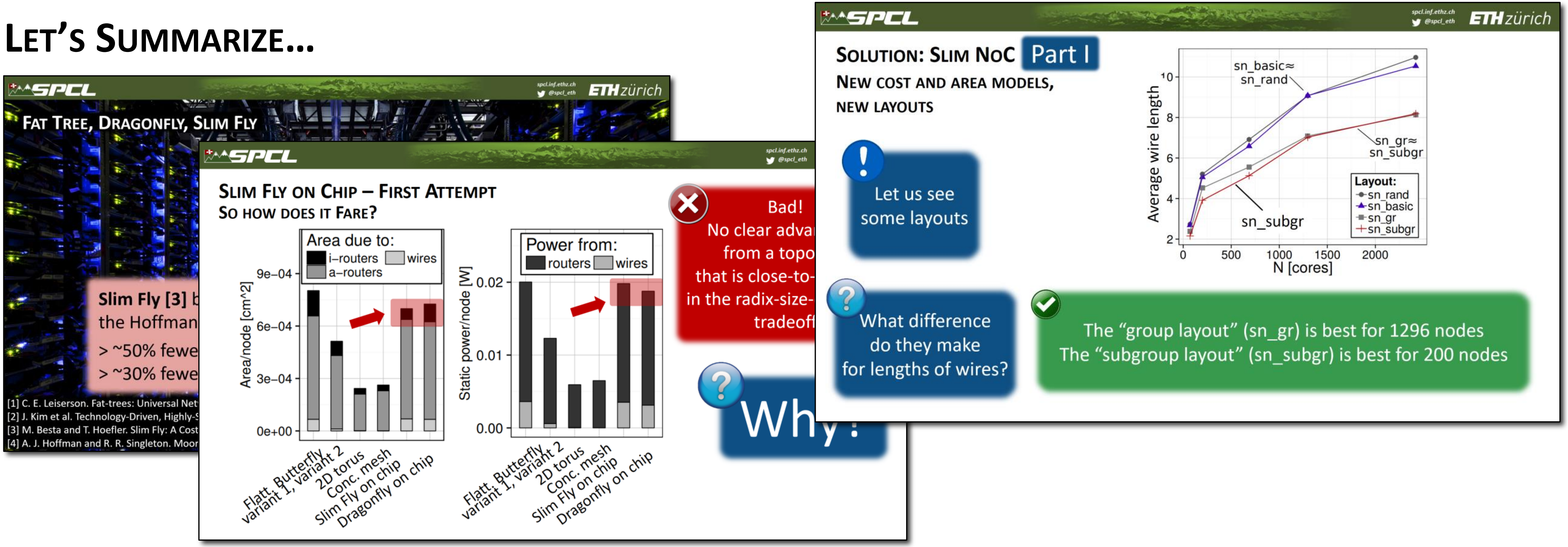

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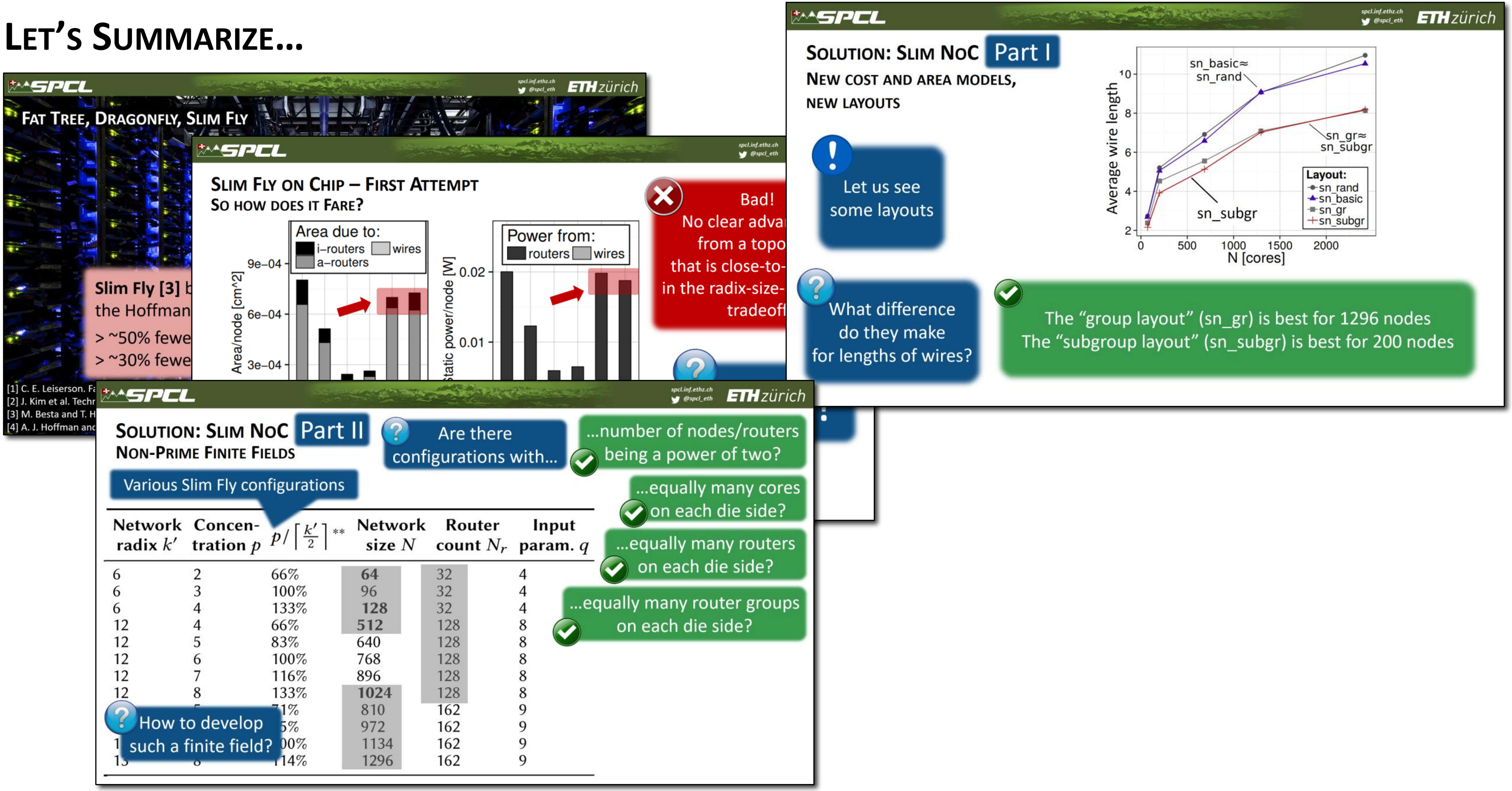

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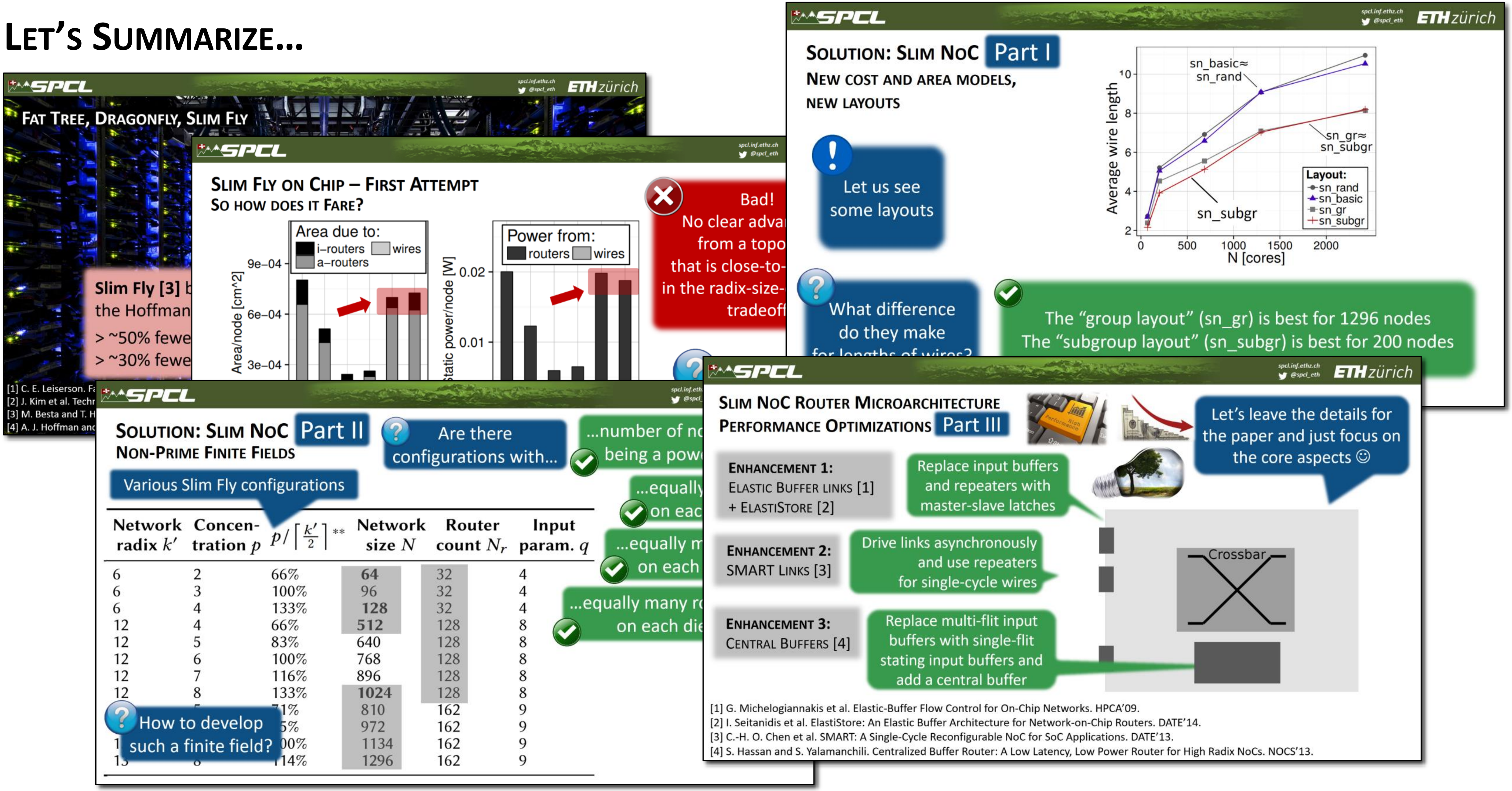
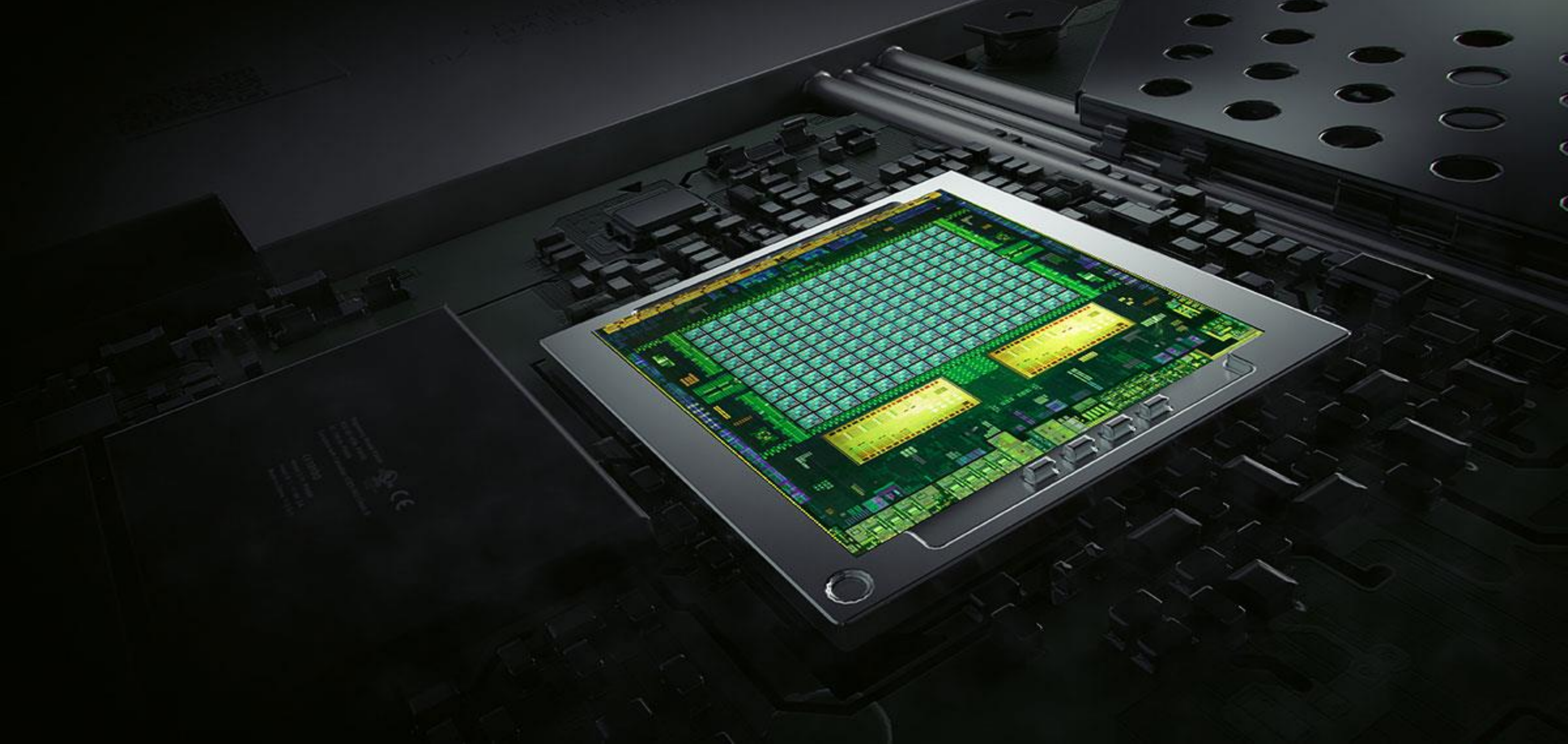


EVALUATION



Evaluation Methodology: Sensitivity Analyses

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- Latency
- Throughput
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- Static/dynamic power consumption
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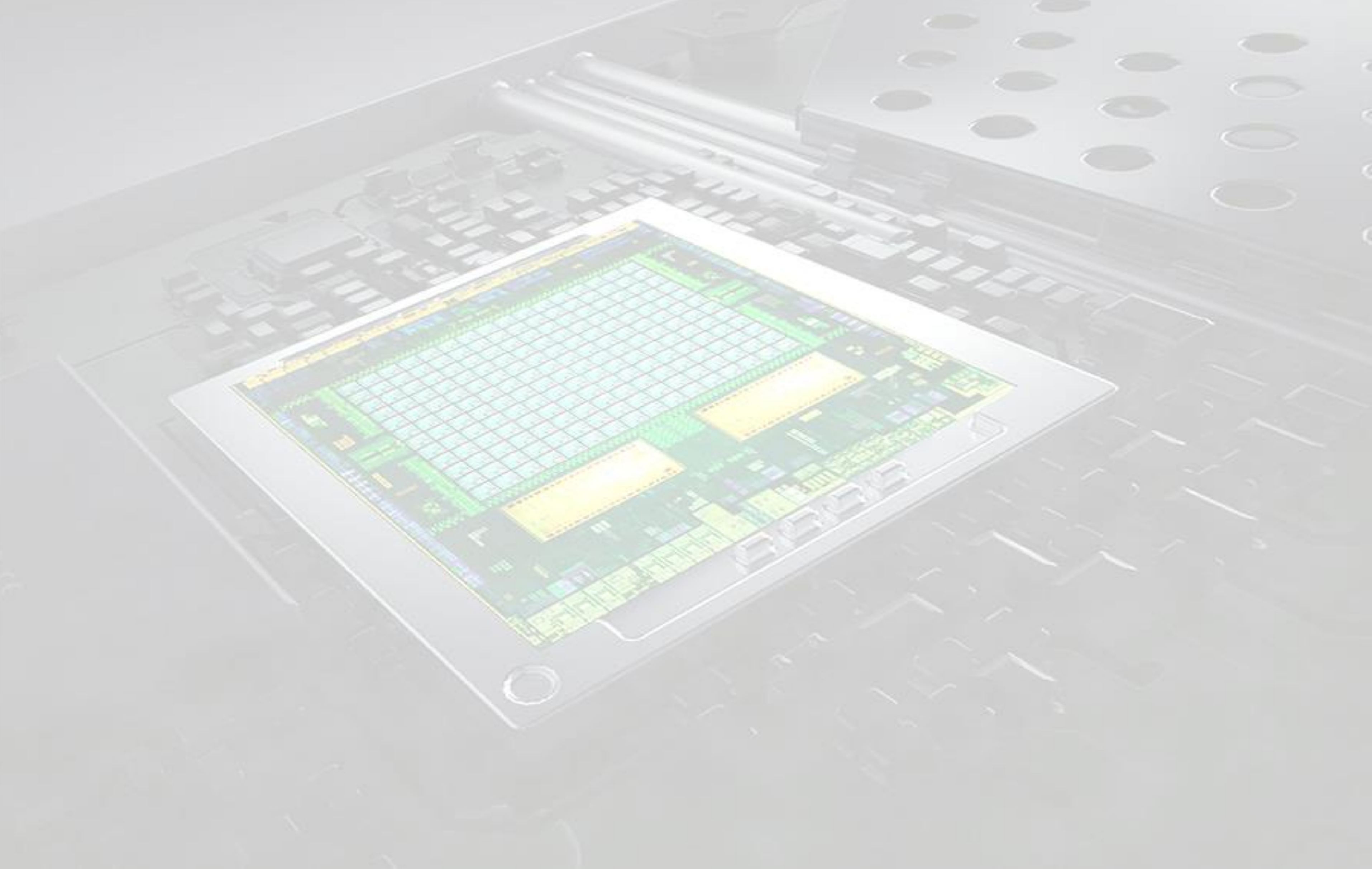
- Bit Shuffle
- Bit Reversal
- Adversarial patterns
- Parsec/Splash traces



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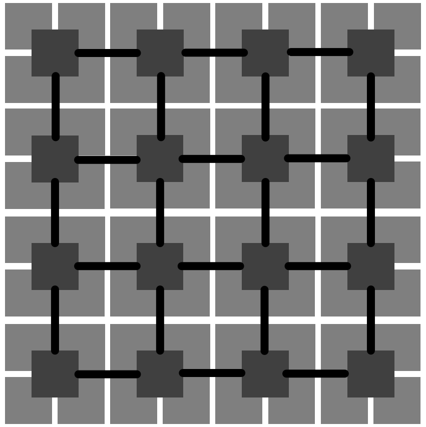

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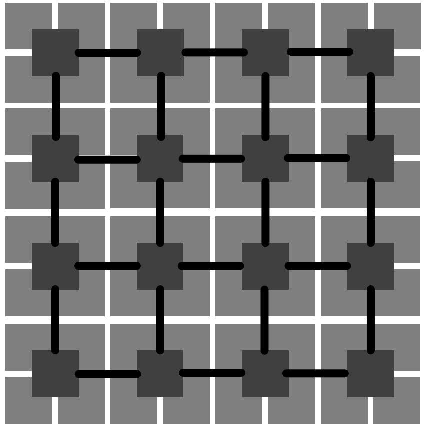
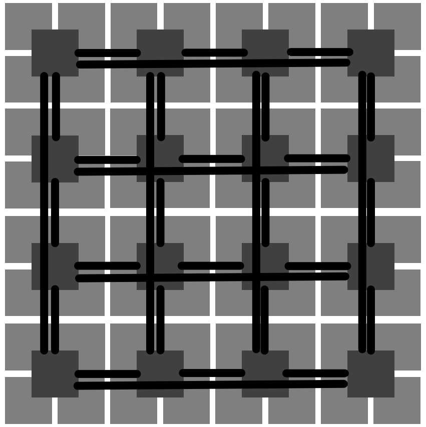


- 2D Torus (T2D)



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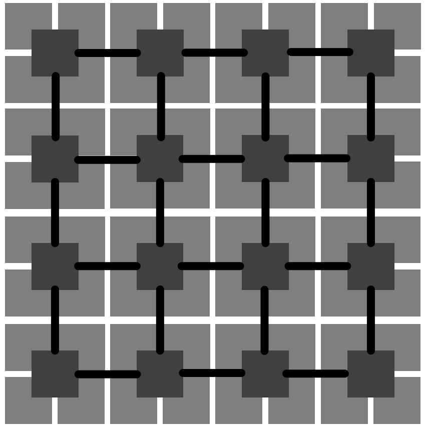
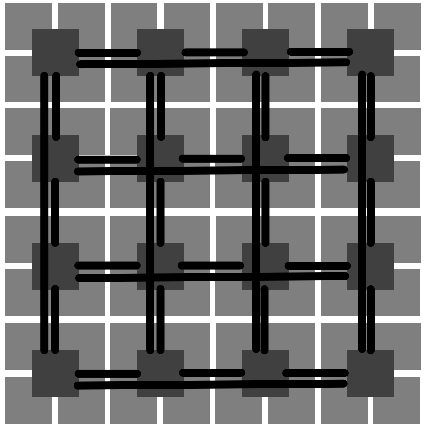
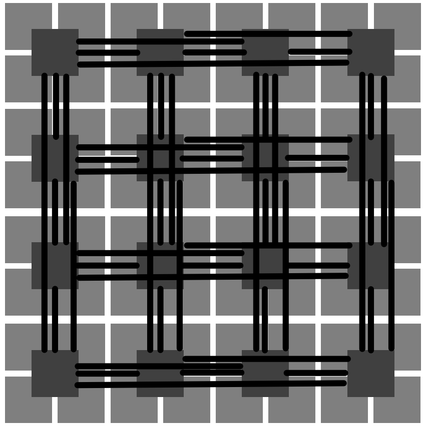


- 2D Torus (T2D)



- Flattened Butterfly [1] (FBF)



[1] J. Kim, W. J. Dally, D. Abts. Flattened butterfly: a cost-efficient topology for high-radix networks. ISCA'07

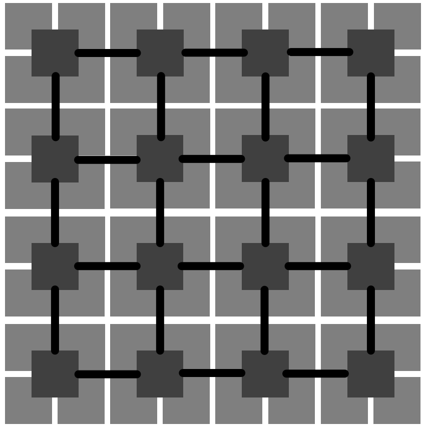
Evaluation Methodology: Sensitivity Analyses

Metrics:
- Latency
- Throughput
- Buffer area
- Buffer size
- Static/dynamic power consumption
- Throughput/power
- Energy-delay product

Traffic / workload:
- Uniform Random
- Bit Shuffle
- Bit Reversal
- Adversarial patterns
- Parsec/Splash traces

Topology:

- Concentrated Mesh (CM)



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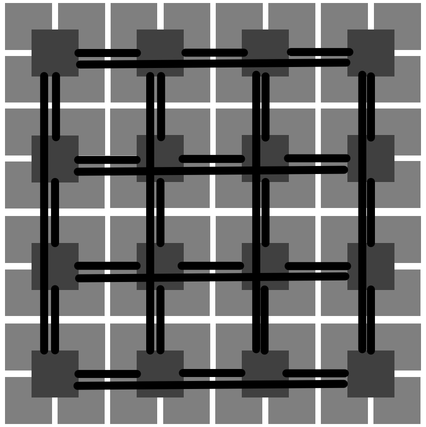

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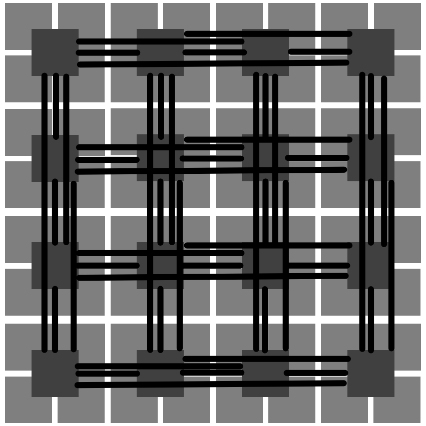
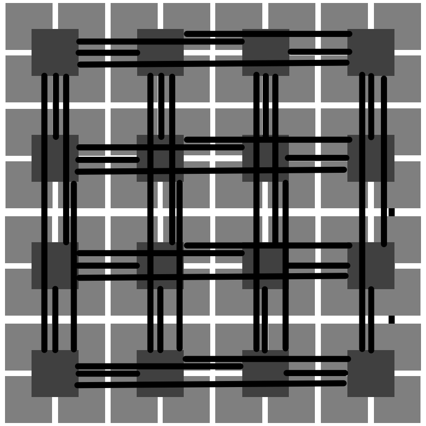


- Flattened Butterfly [1], a „Partitioned” Variant (PFBF)



[1] J. Kim, W. J. Dally, D. Abts. Flattened butterfly: a cost-efficient topology for high-radix networks. ISCA’07

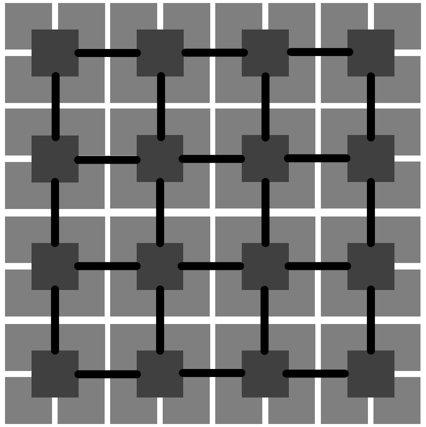
Evaluation Methodology: Sensitivity Analyses

Metrics:
- Latency
- Throughput
- Buffer area
- Buffer size
- Static/dynamic power consumption
- Throughput/power
- Energy-delay product

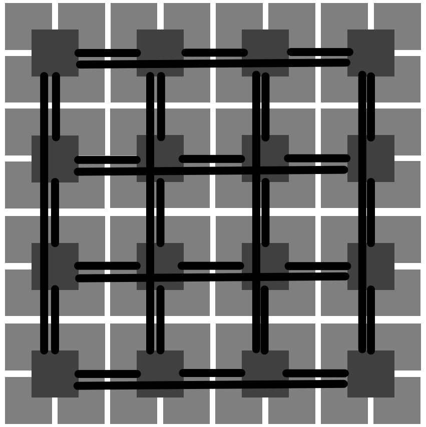
Traffic / workload:
- Uniform Random
- Bit Shuffle
- Bit Reversal
- Adversarial patterns
- PARSEC/SPLASH traces

Topology:

- Concentrated Mesh (CM)



- 2D Torus (T2D)



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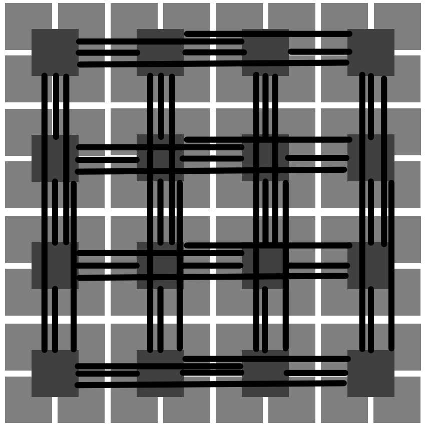
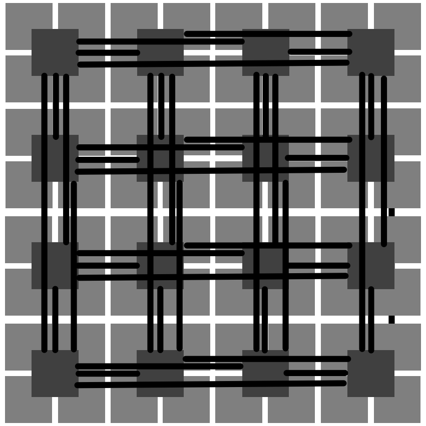


- Flattened Butterfly [1], a „partitioned" variant (PFBF)



- (Briefly) hierarchical NoCs

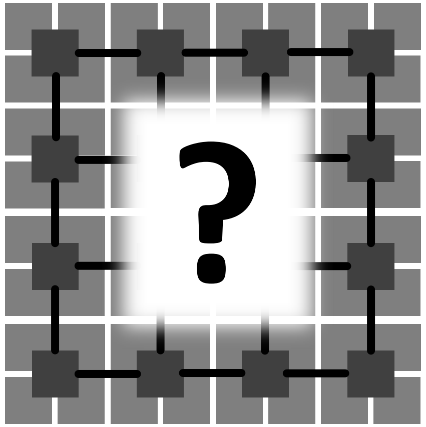
[1] J. Kim, W. J. Dally, D. Abts. Flattened butterfly: a cost-efficient topology for high-radix networks. ISCA'07

Evaluation Methodology: Sensitivity Analyses

Evaluation Methodology: Sensitivity Analyses

Layout:

- Group
- Subgroup
- Random
- Naive



Evaluation Methodology: Sensitivity Analyses

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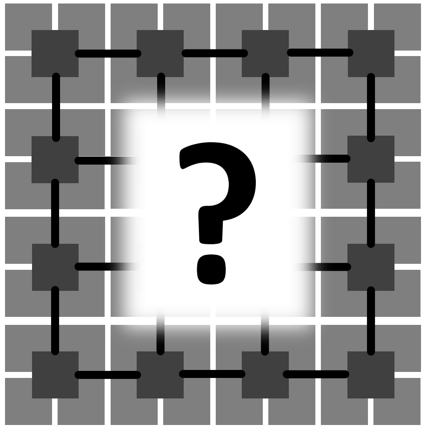
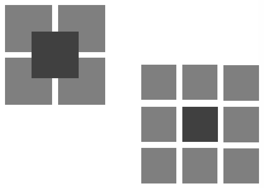
- Group
- Subgroup
- Random
- Naive

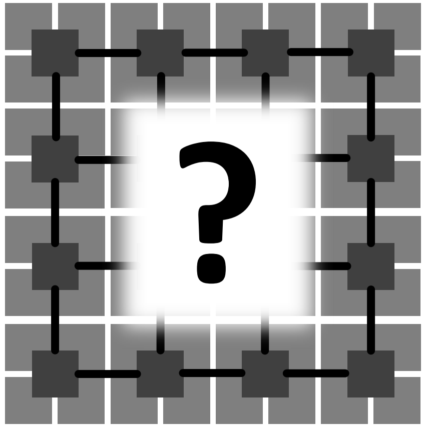


Concentration:
- 3
- 4
- 8
- 9

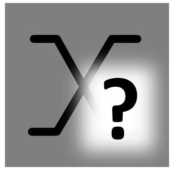


Evaluation Methodology: Sensitivity Analyses

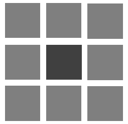
Layout:
- Group
- Subgroup
- Random
- Naive



Router cycle time:
- 0.4ns
- 0.5ns
- 0.6ns



Concentration:
- 3
- 4
- 8
- 9

Evaluation Methodology: Sensitivity Analyses

Layout:
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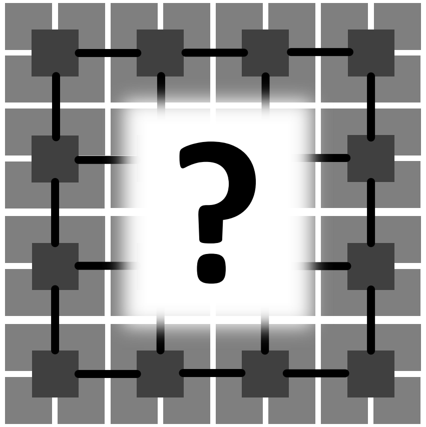

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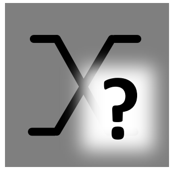
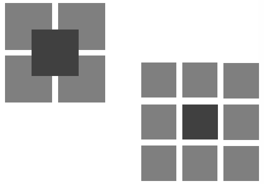


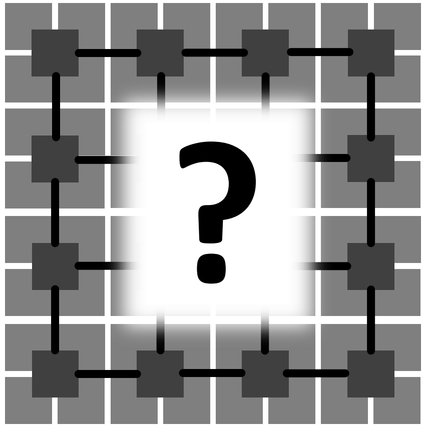
Technology node:
- 22nm
- 45nm

Concentration:
- 3
- 4
- 8
- 9



Evaluation Methodology: Sensitivity Analyses

Layout:
- Group
- Subgroup
- Random
- Naive



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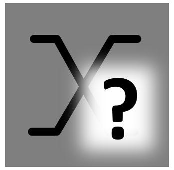

Technology node:
- 22nm
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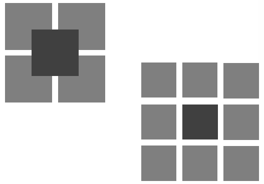
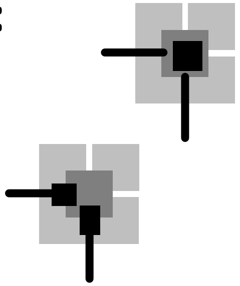
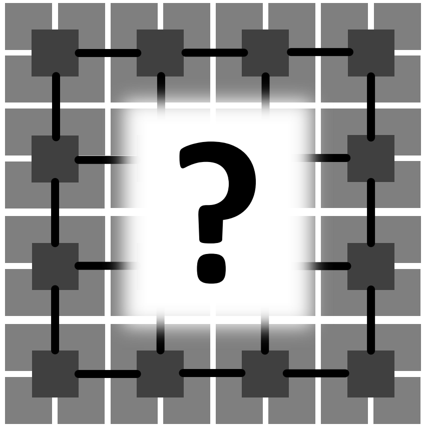


Buffer type:
- Central
- Edge



Evaluation Methodology: Sensitivity Analyses

Layout:
- Group
- Subgroup
- Random
- Naive



Router cycle time:
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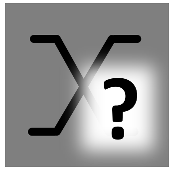
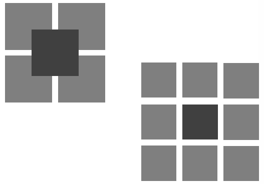
- 0.6ns



Injection rate:
- 0.01 – 0.95

Technology node:
- 22nm
- 45nm

Concentration:
- 3
- 4
- 8
- 9



Buffer type:
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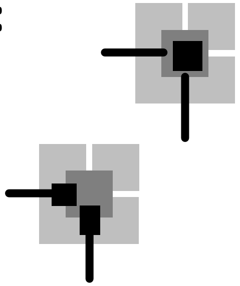
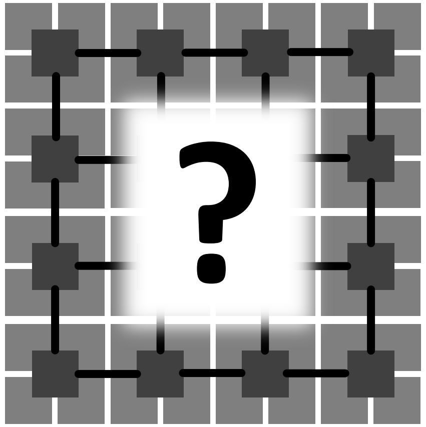


Evaluation Methodology: Sensitivity Analyses

Layout:
- Group
- Subgroup
- Random
- Naive



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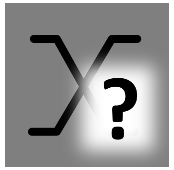

Injection rate:
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Technology node:
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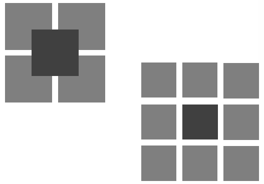
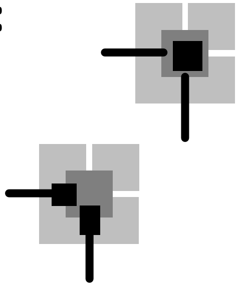


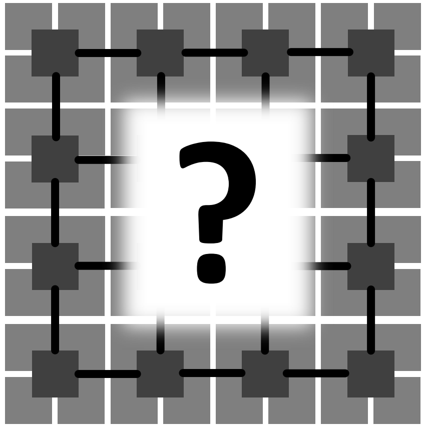
Buffer type:
- Central
- Edge



Microarchitecture enhancement:
- SMART ON/OFF
- Central Buffers ON/OFF

Evaluation Methodology: Sensitivity Analyses

Layout:
- Group
- Subgroup
- Random
- Naive



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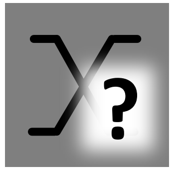
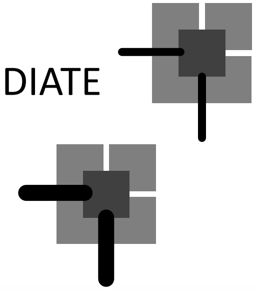


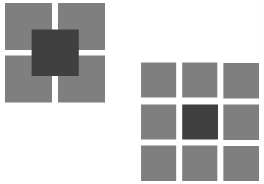
Injection rate:
- 0.01 – 0.95

Technology node:
- 22nm
- 45nm

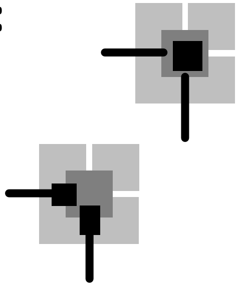
Wire type:
- Intermediate
- Global



Concentration:
- 3
- 4
- 8
- 9



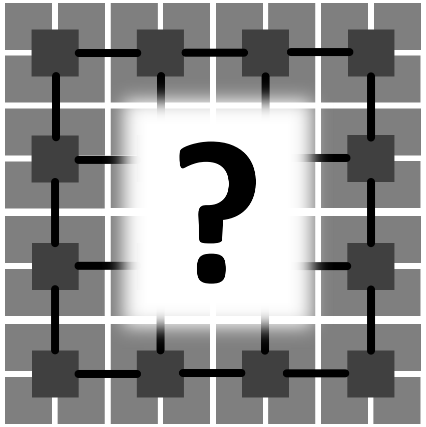
Buffer type:
- Central
- Edge



Microarchitecture enhancement:
- SMART ON/OFF
- Central Buffers ON/OFF

Evaluation Methodology: Sensitivity Analyses

Layout:
- Group
- Subgroup
- Random
- Naive



Router cycle time:
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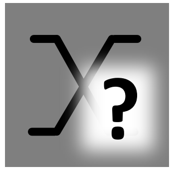
- 0.5ns
- 0.6ns



Injection rate:
- 0.01 – 0.95

Technology node:
- 22nm
- 45nm

Wire type:
- Intermediate
- Global

Network size (Node count):
- 200
- 1024
- 1296

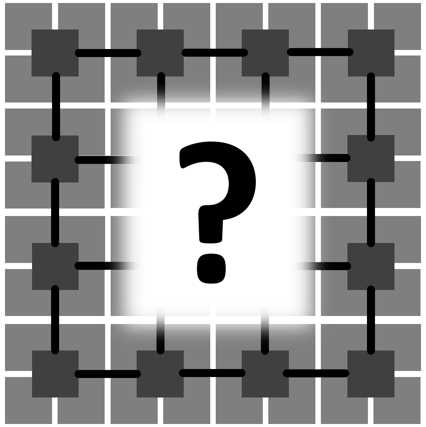
Concentration:
- 3
- 4
- 8
- 9

Buffer type:
- Central
- Edge

Microarchitecture enhancement:
- SMART ON/OFF
- Central Buffers ON/OFF

Evaluation Methodology: Sensitivity Analyses

Layout:
- Group
- Subgroup
- Random
- Naive



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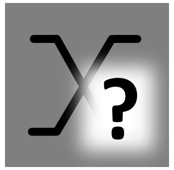
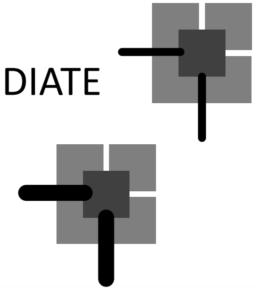


Routing
- Minimum static
- Non-minimum adaptive

Injection rate:
- 0.01 – 0.95

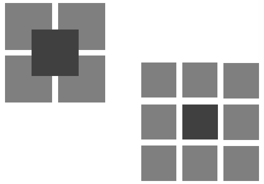
Technology node:
- 22nm
- 45nm

Wire type:
- Intermediate
- Global

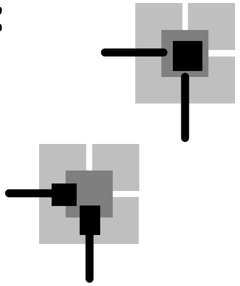


Network size (Node count):
- 200
- 1024
- 1296

Concentration:
- 3
- 4
- 8
- 9



Buffer type:
- Central
- Edge



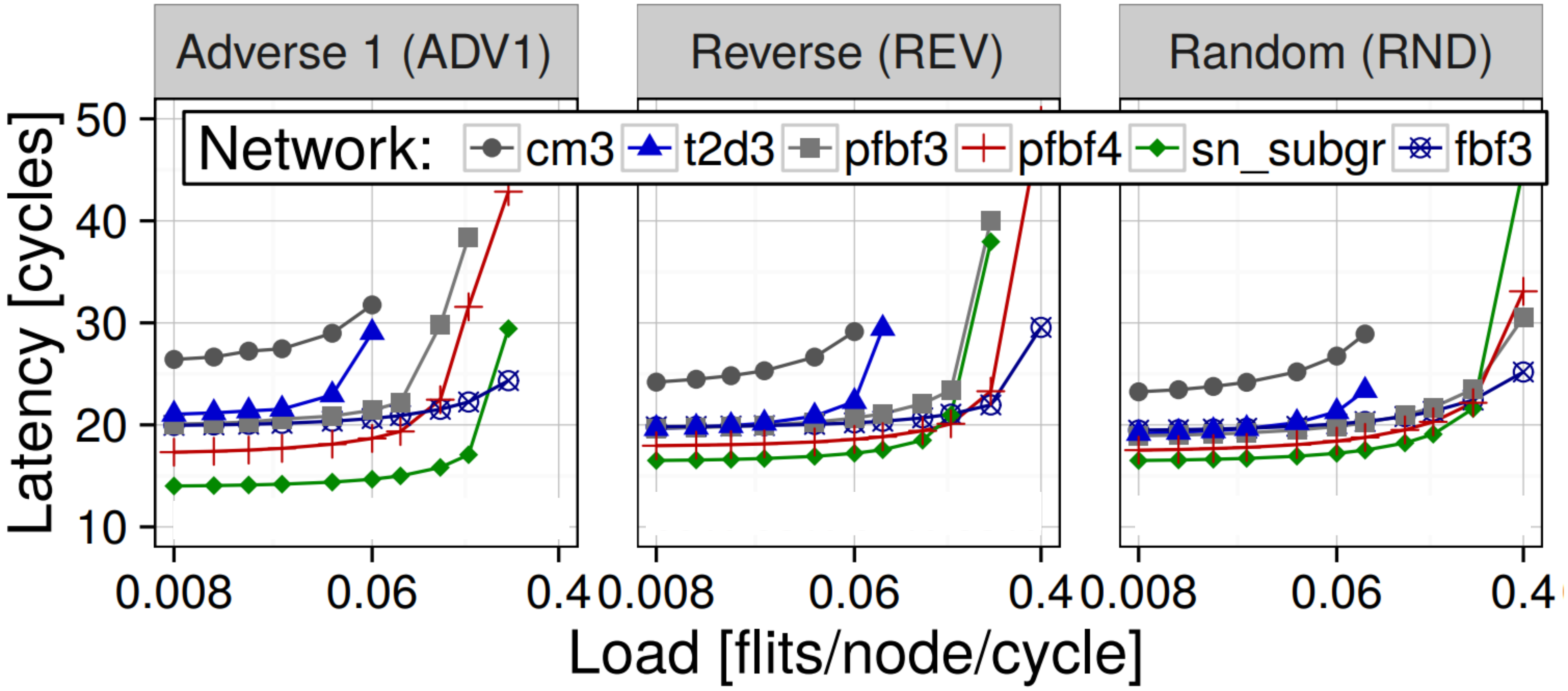
Microarchitecture enhancement:
- SMART ON/OFF
- Central Buffers ON/OFF

RESULTS: PERFORMANCE

in-house simulator [1]

cm3: concentrated mesh, **t2d3**: torus, **pfbf3**, **pfbf4**, **fbf3**: variants of Flattened Butterfly, **sn_subgr**: Slim NoC (the subgroup layout)

SMART LINKS: ON
CENTRAL BUFFERS: ON
NODE COUNT: 192/200



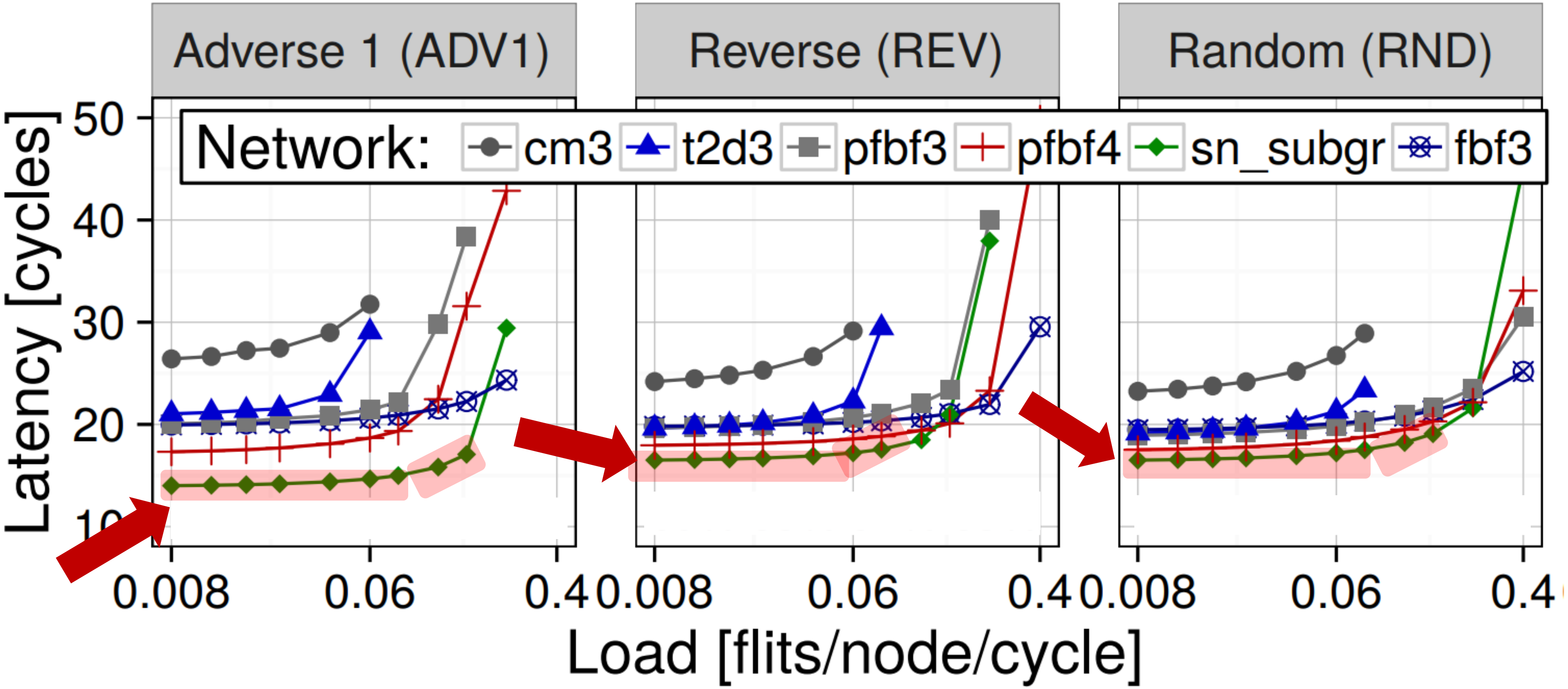
[1] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.

RESULTS: PERFORMANCE

in-house simulator [1]

cm3: concentrated mesh, **t2d3**: torus, **pfbf3**, **pfbf4**, **fbf3**: variants of Flattened Butterfly, **sn_subgr**: Slim NoC (the subgroup layout)

SMART LINKS: ON
CENTRAL BUFFERS: ON
NODE COUNT: 192/200



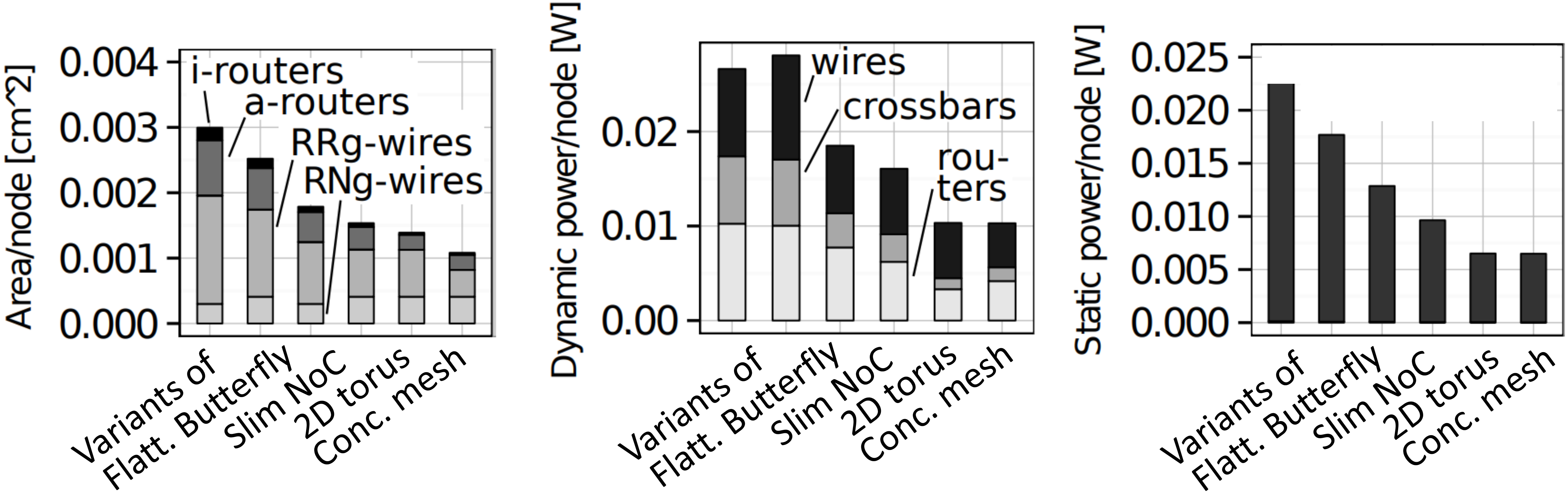
Slim NoC provides the lowest latency

[1] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.

SMART LINKS: ON CENTRAL BUFFERS: ON
NODE COUNT: 192/200, TECHNOLOGY NODE: 45NM

RESULTS: AREA AND POWER CONSUMPTION

DSENT power simulator [1]



i-routers: routers (intermediate layer), **a-routers**: routers (active layer),
RRg-wires: router-router wires (global layer), **RNg-wires**: router-node wires (global layer).

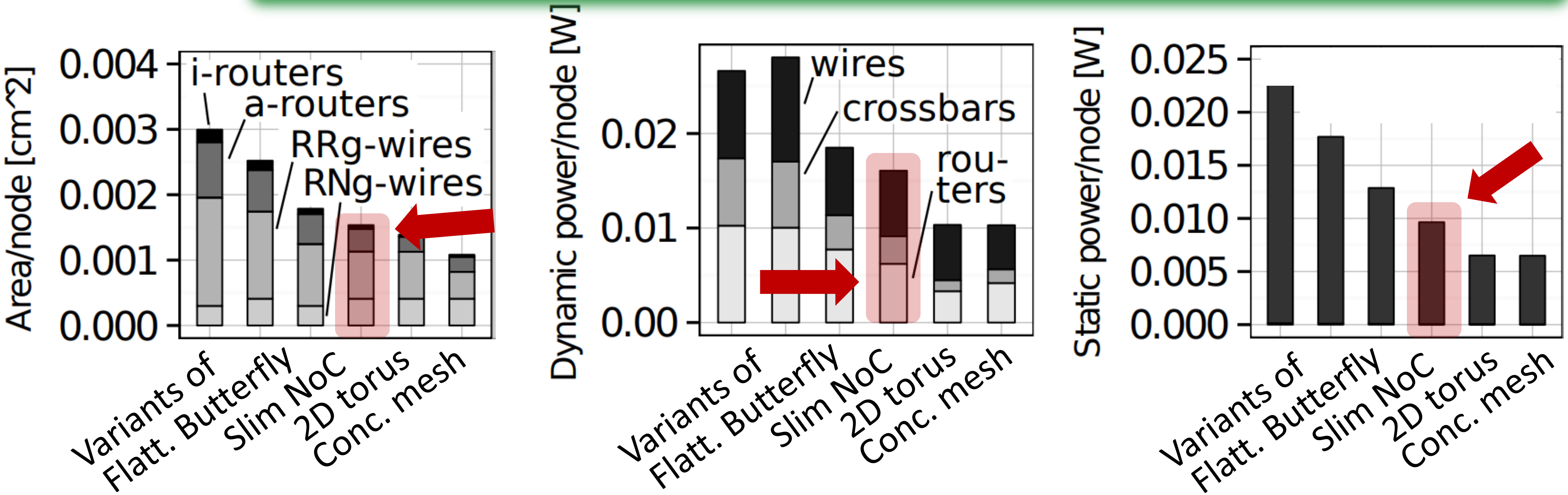
[1] C. Sun et al. DSENT - A Tool Connecting Emerging Photonics with Electronics for Opto-Electronic Networks-on-Chip Modeling. NOCS’12.

SMART LINKS: ON CENTRAL BUFFERS: ON
NODE COUNT: 192/200, TECHNOLOGY NODE: 45NM

RESULTS: AREA AND POWER CONSUMPTION

DSENT power simulator [1]

Slim NoC is more efficient than high-radix designs



i-routers: routers (intermediate layer), **a-routers**: routers (active layer),
RRg-wires: router-router wires (global layer), **RNg-wires**: router-node wires (global layer).

[1] C. Sun et al. DSENT - A Tool Connecting Emerging Photonics with Electronics for Opto-Electronic Networks-on-Chip Modeling. NOCS'12.

RESULTS: THROUGHPUT / POWER (PARSEC/SPLASH)

in-house simulator [1]

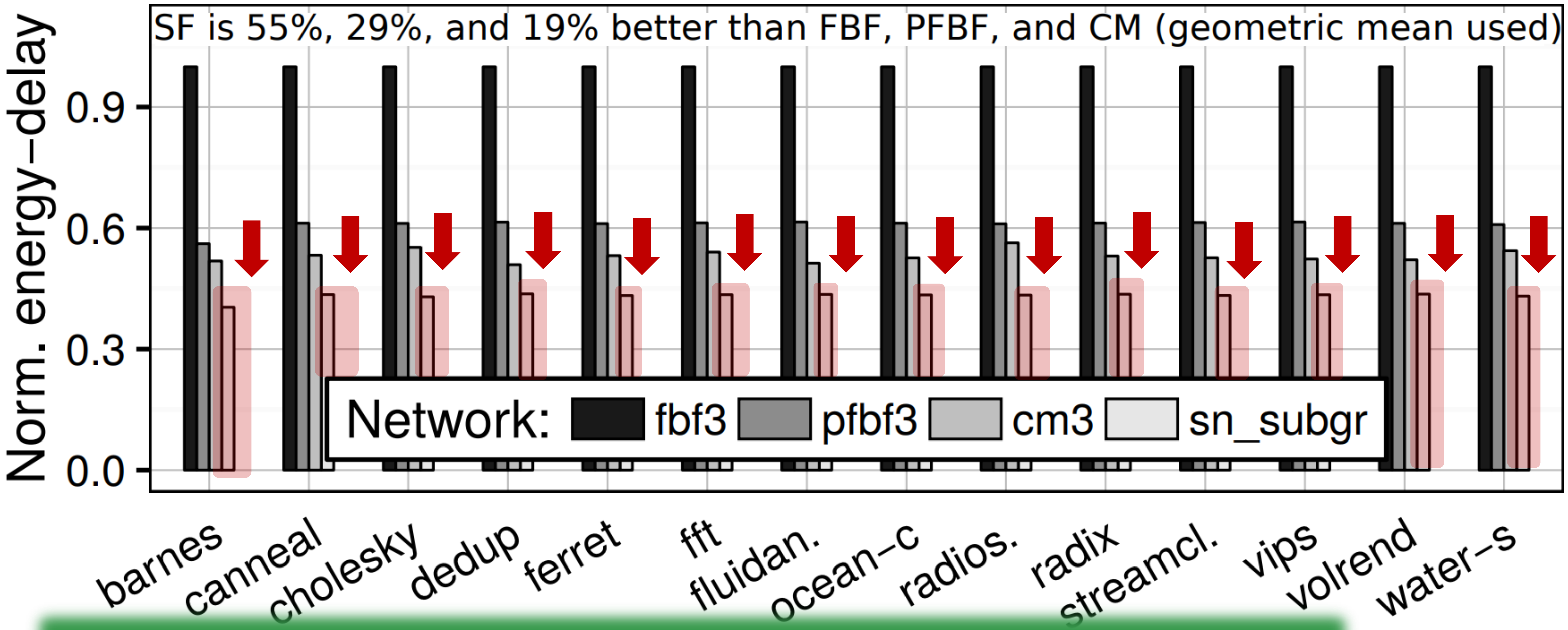
SMART LINKS: ON
CENTRAL BUFFERS: ON
NODE COUNT: 192/200

[1] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.

Results: Throughput / Power (PARSEC/SPLASH)

in-house simulator [1]

SMART links: ON
Central Buffers: ON
Node count: 192/200



Slim NoC provides a power-performance sweetspot

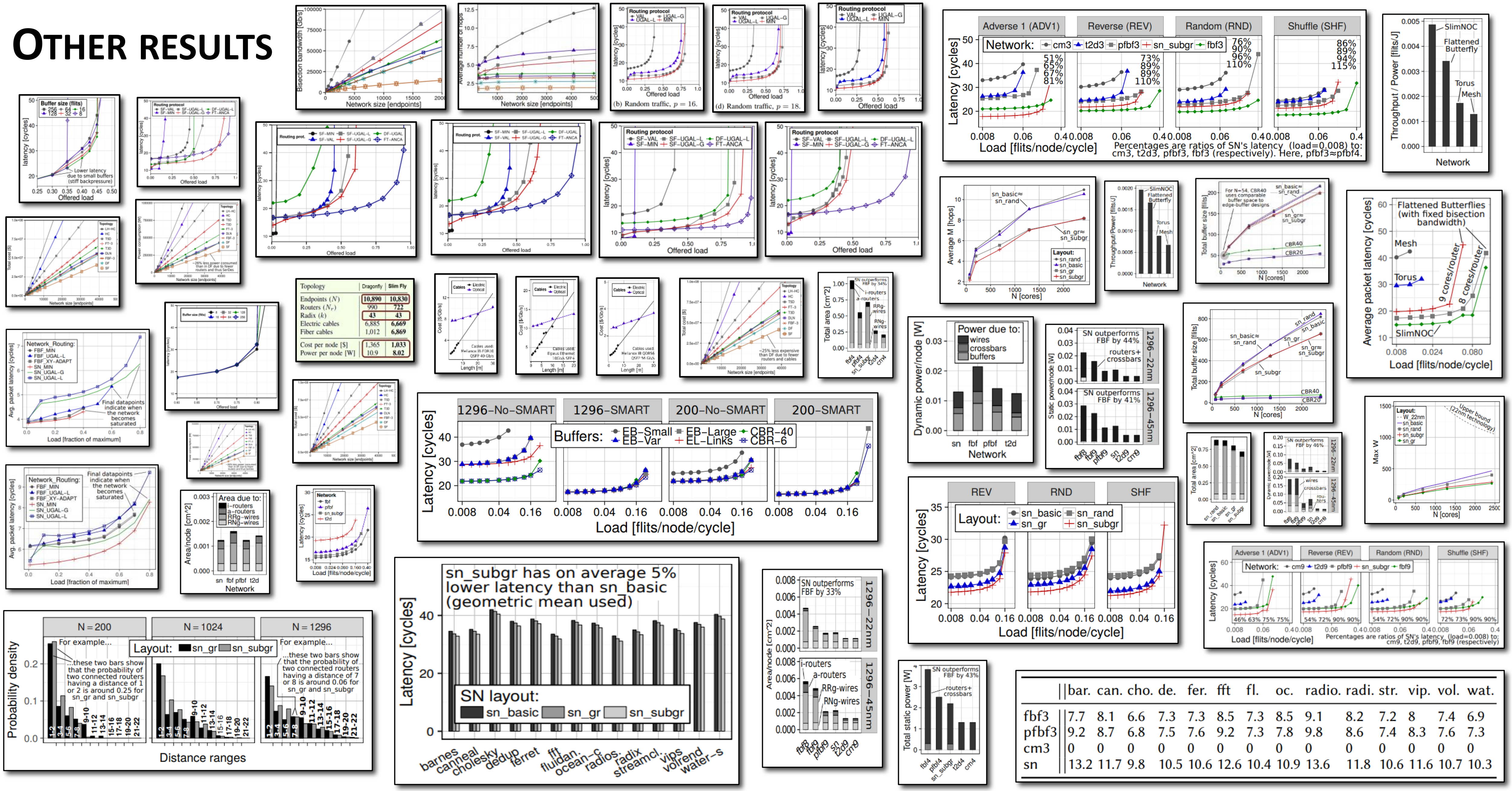
[1] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.

RESULTS: SCALABILITY

Slim NoC is similarly advantageous
when we move
from 200 nodes to 1296 nodes
(check the paper for details ☺)

Other results

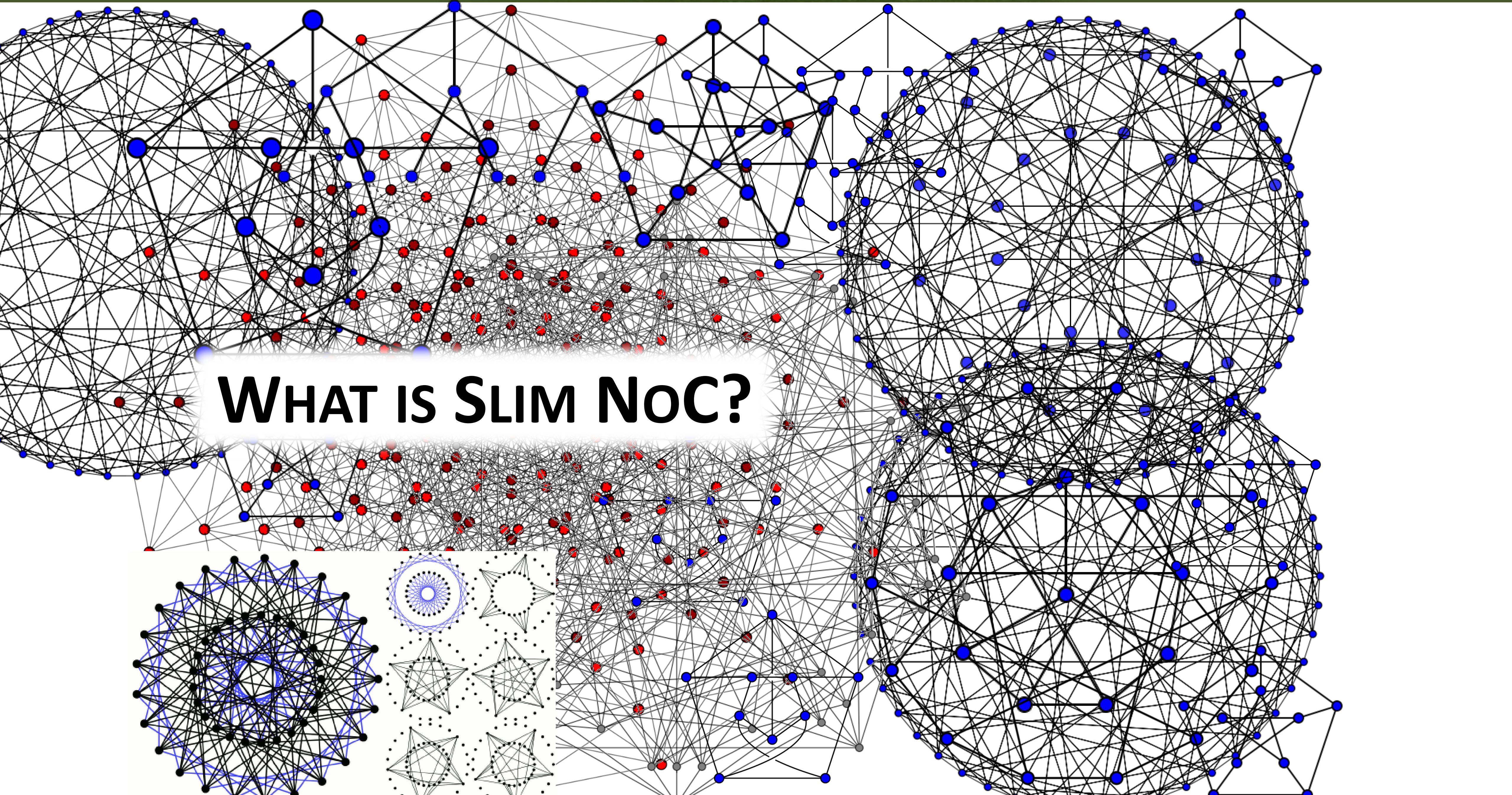
OTHER RESULTS



Topology	Dragonfly	Slim Fly
Endpoints (N)	10,890	10,830
Routers (N_r)	990	722
Radix (k)	43	43
Electric cables	6,885	6,669
Fiber cables	1,012	6,869
Cost per node [$]	1,365	1,033
Power per node [W]	10.9	8.02

	bar.	can.	cho.	de.	fer.	fft	fl.	oc.	radio.	radi.	str.	vip.	vol.	wat.
fbf3	7.7	8.1	6.6	7.3	7.3	8.5	7.3	8.5	9.1	8.2	7.2	8	7.4	6.9
pfbf3	9.2	8.7	6.8	7.5	7.6	9.2	7.3	7.8	9.8	8.6	7.4	8.3	7.6	7.3
cm3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
sn	13.2	11.7	9.8	10.5	10.6	12.6	10.4	10.9	13.6	11.8	10.6	11.6	10.7	10.3

What is Slim NoC?



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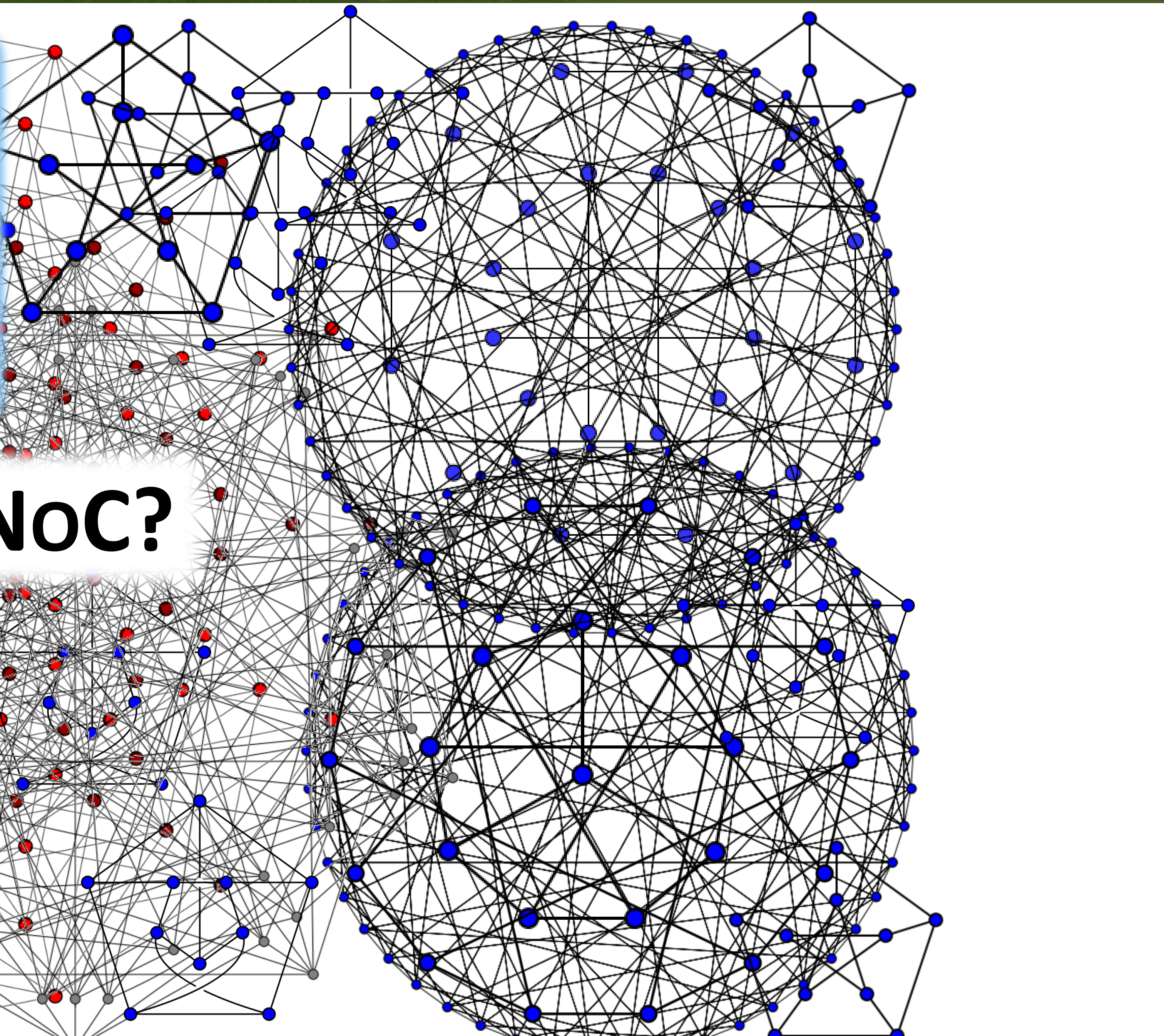
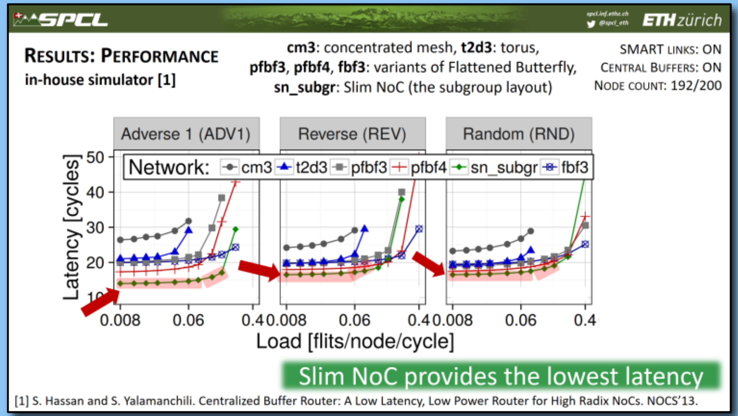


A low-latency topology



Results: Performance
in-house simulator [1]

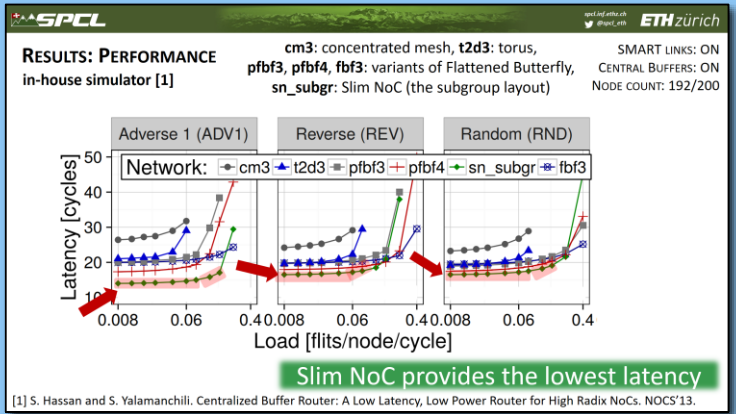
cm3: concentrated mesh, **t2d3**: torus,
pfbf3, **pfbf4**, **fbf3**: variants of Flattened Butterfly,
sn_subgr: Slim NoC (the subgroup layout)

Smart links: ON
Central Buffers: ON
Node count: 192/200

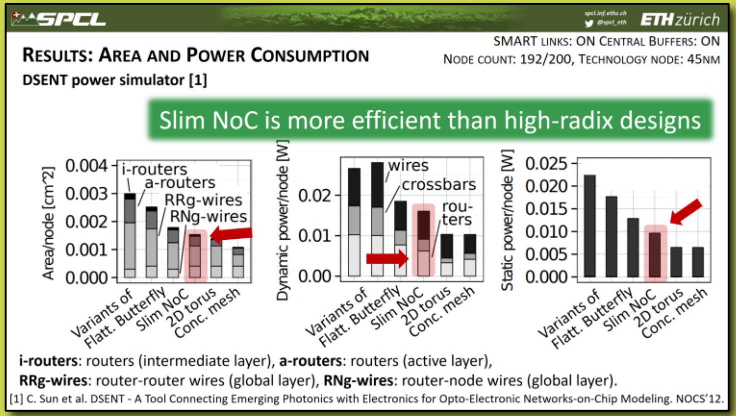
Slim NoC provides the lowest latency

[1] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.

A low-latency topology



An area- and energy-efficient topology



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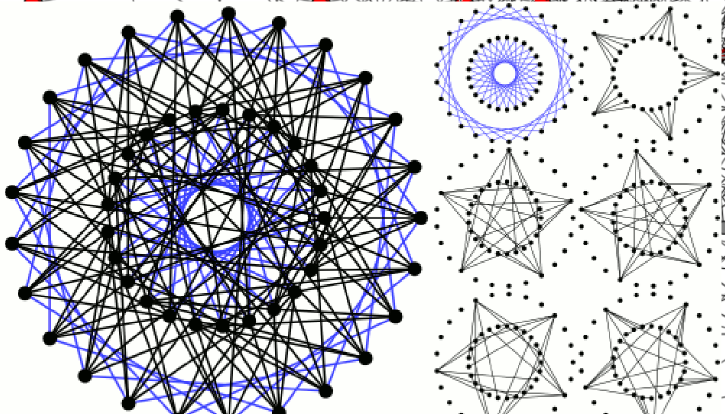

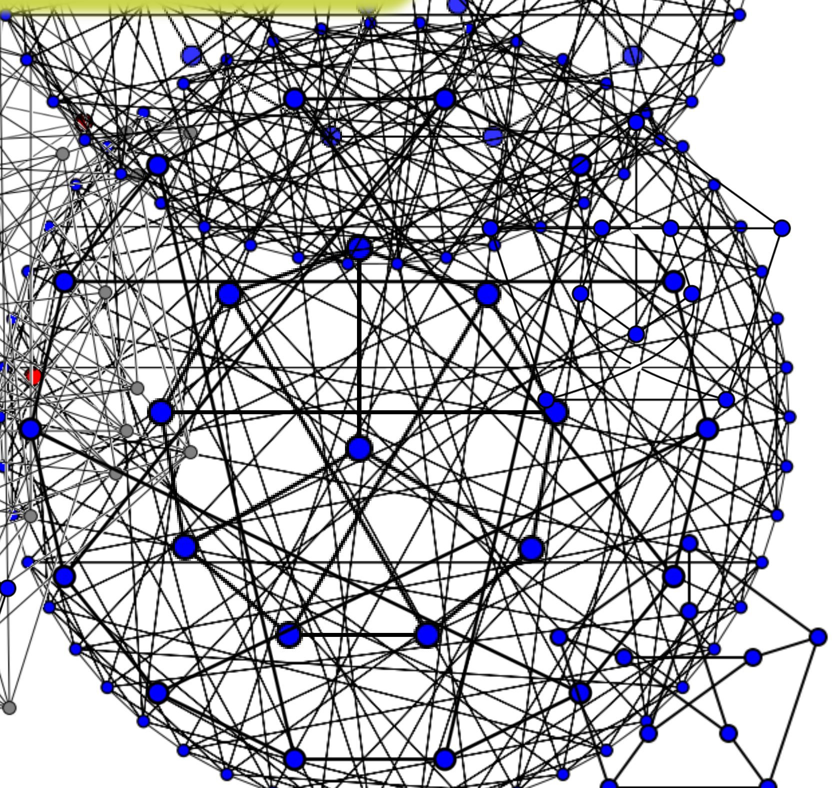

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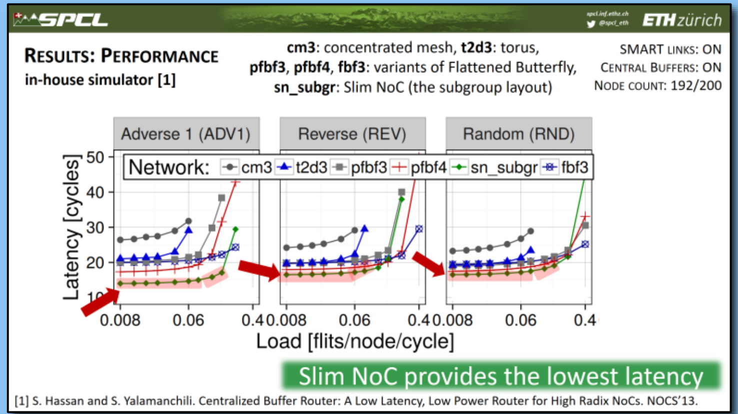

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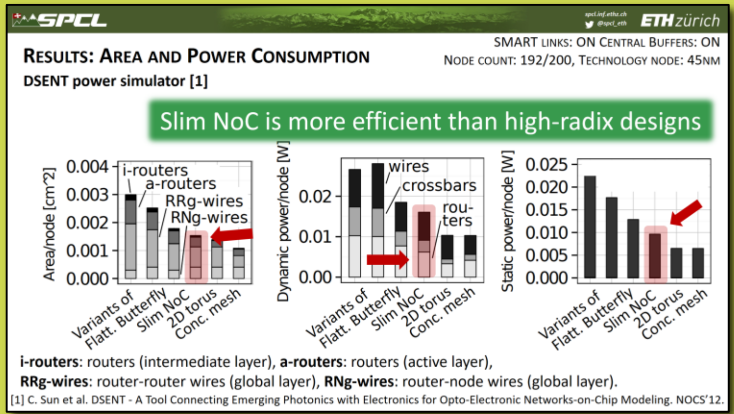
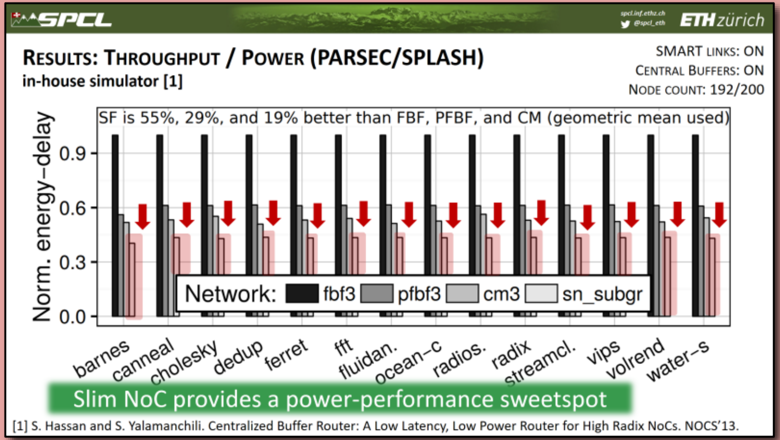


What is Slim NoC?

A power-performance-sweetspot topology



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What is Slim NoC?

A low-latency topology

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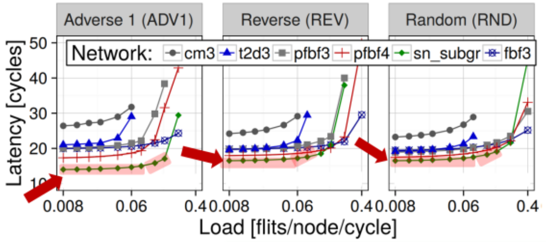


Slim NoC provides the lowest latency

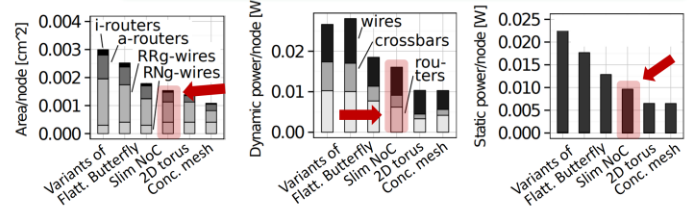
[1] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.

An area- and energy-efficient topology

Results: Area and Power Consumption
DSENT power simulator [1]

SMART links: ON Central Buffers: ON
Node count: 192/200, Technology node: 45nm

Slim NoC is more efficient than high-radix designs



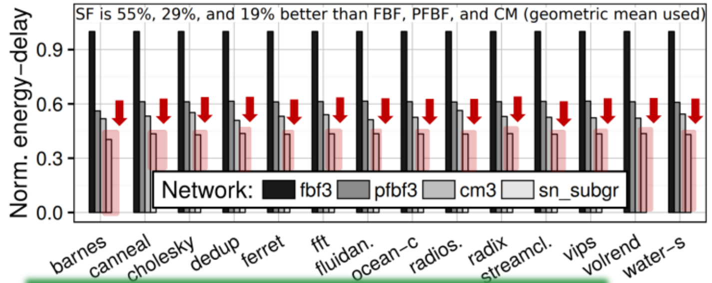
i-routers: routers (intermediate layer), **a-routers**: routers (active layer),
RRg-wires: router-router wires (global layer), **RNg-wires**: router-node wires (global layer).

[1] C. Sun et al. DSENT - A Tool Connecting Emerging Photonics with Electronics for Opto-Electronic Networks-on-Chip Modeling. NOCS'12.

A power-performance-sweetspot topology

Results: Throughput / Power (PARSEC/SPLASH)
in-house simulator [1]

SMART links: ON
Central Buffers: ON
Node count: 192/200

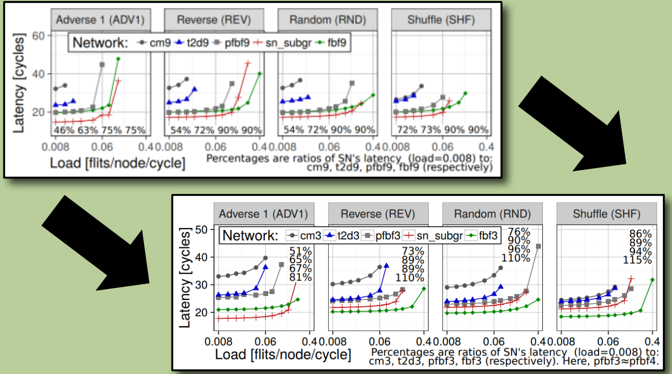


Slim NoC provides a power-performance sweetspot

[1] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.

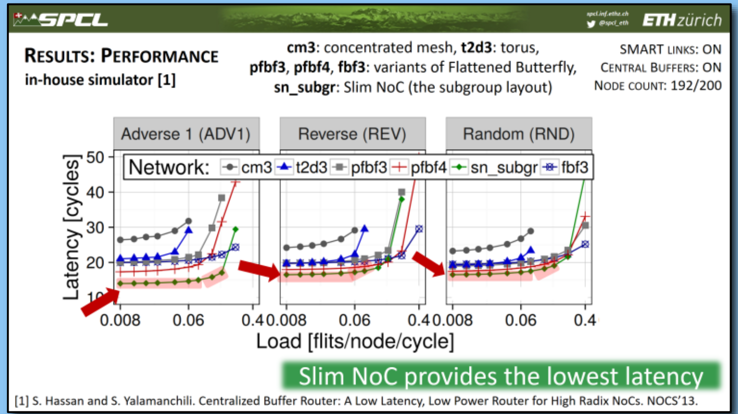
A highly-scalable topology

200 nodes

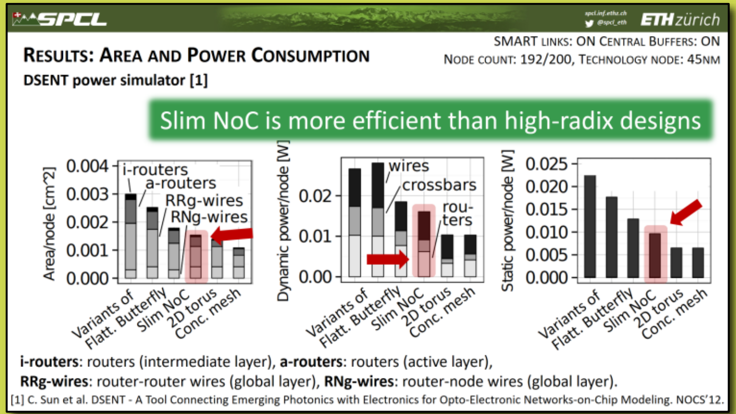


1296 nodes

A low-latency topology



An area- and energy-efficient topology

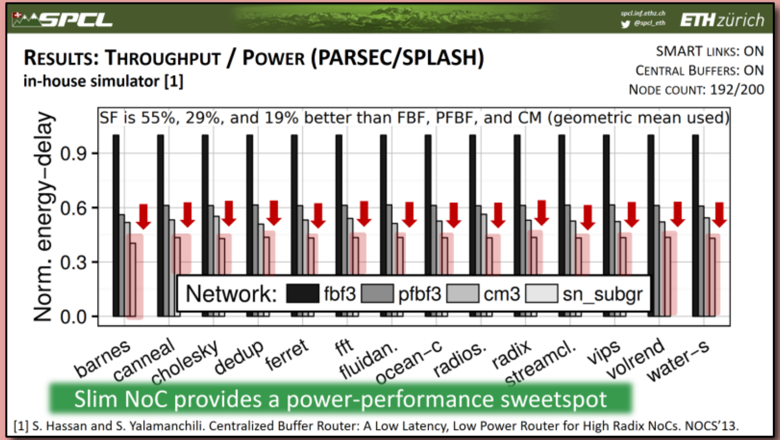


Website:

http://spcl.inf.ethz.ch/Research/Scalable_Networking/SlimNoC

What is Slim NoC?

A power-performance-sweetspot topology



A highly-scalable topology

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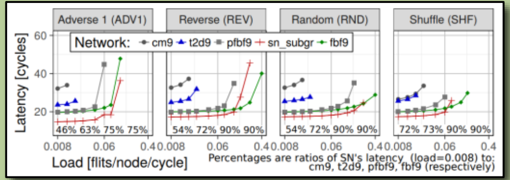
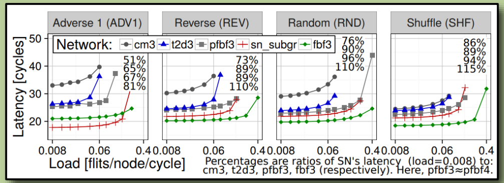
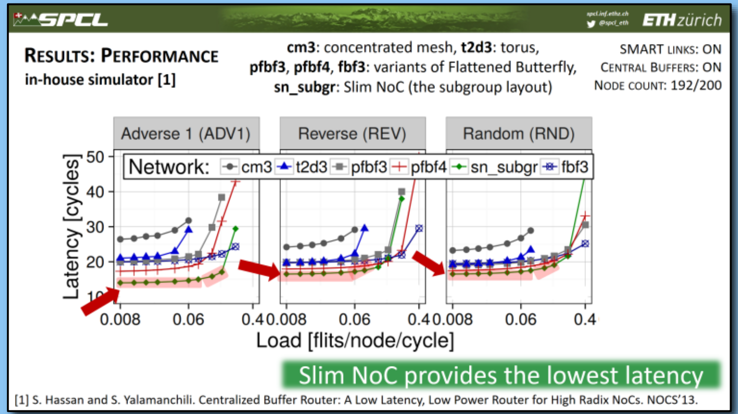




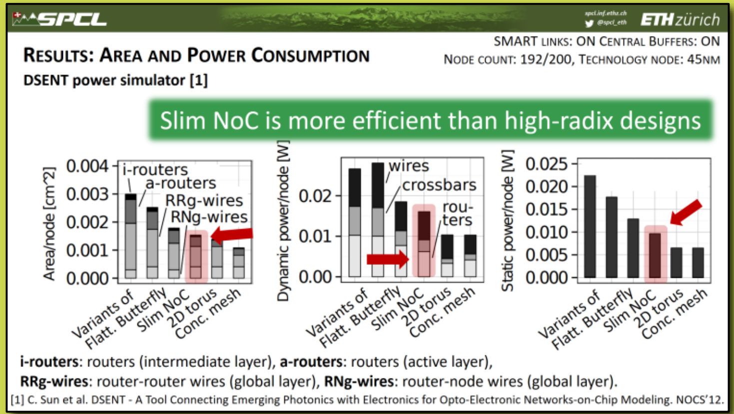
1296 nodes

What is Slim NoC?

A low-latency topology



An area- and energy-efficient topology



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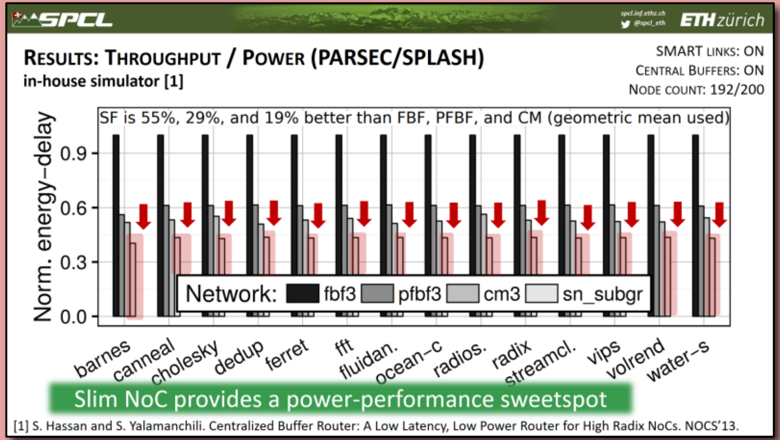
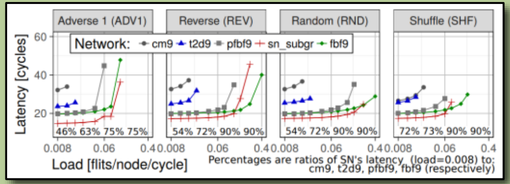
COMING SOON

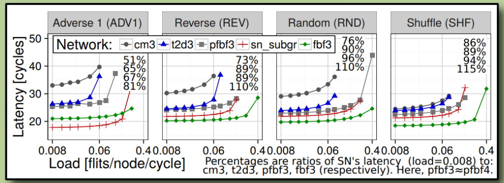
A power-performance-sweetspot topology



A highly-scalable topology

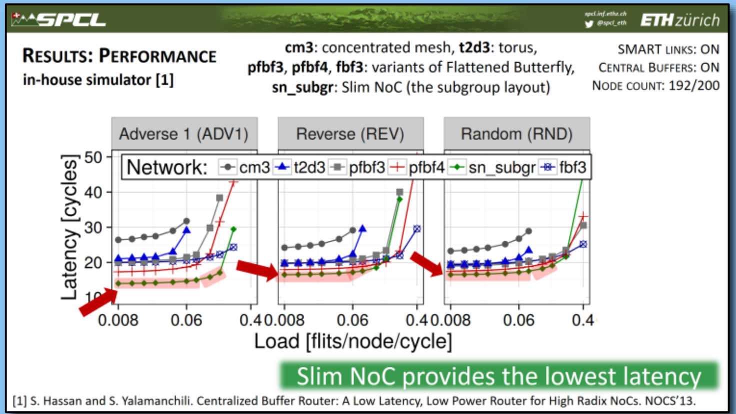
200 nodes



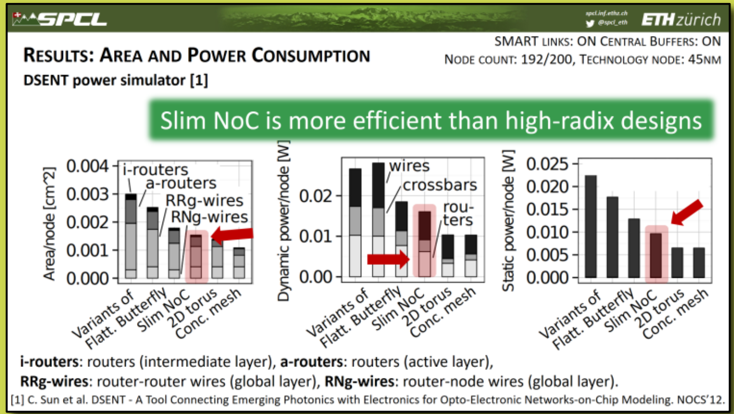


1296 nodes

A LOW-LATENCY TOPOLOGY



AN AREA- AND ENERGY-EFFICIENT TOPOLOGY



Website:

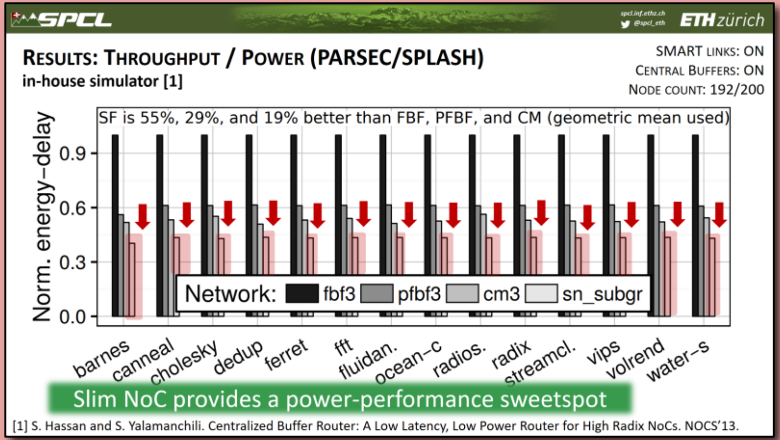
http://spcl.inf.ethz.ch/Research/Scalable_Networking/SlimNoC

WHAT IS SLIM NOC?

Thank you for your attention

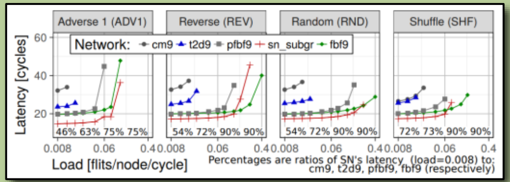
COMING SOON

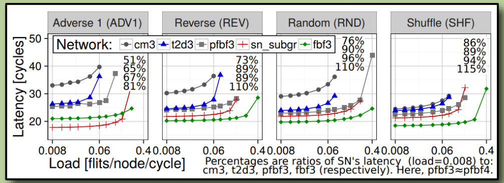
A POWER-PERFORMANCE-SWEETSPOT TOPOLOGY



A HIGHLY-SCALABLE TOPOLOGY

200 nodes





1296 nodes

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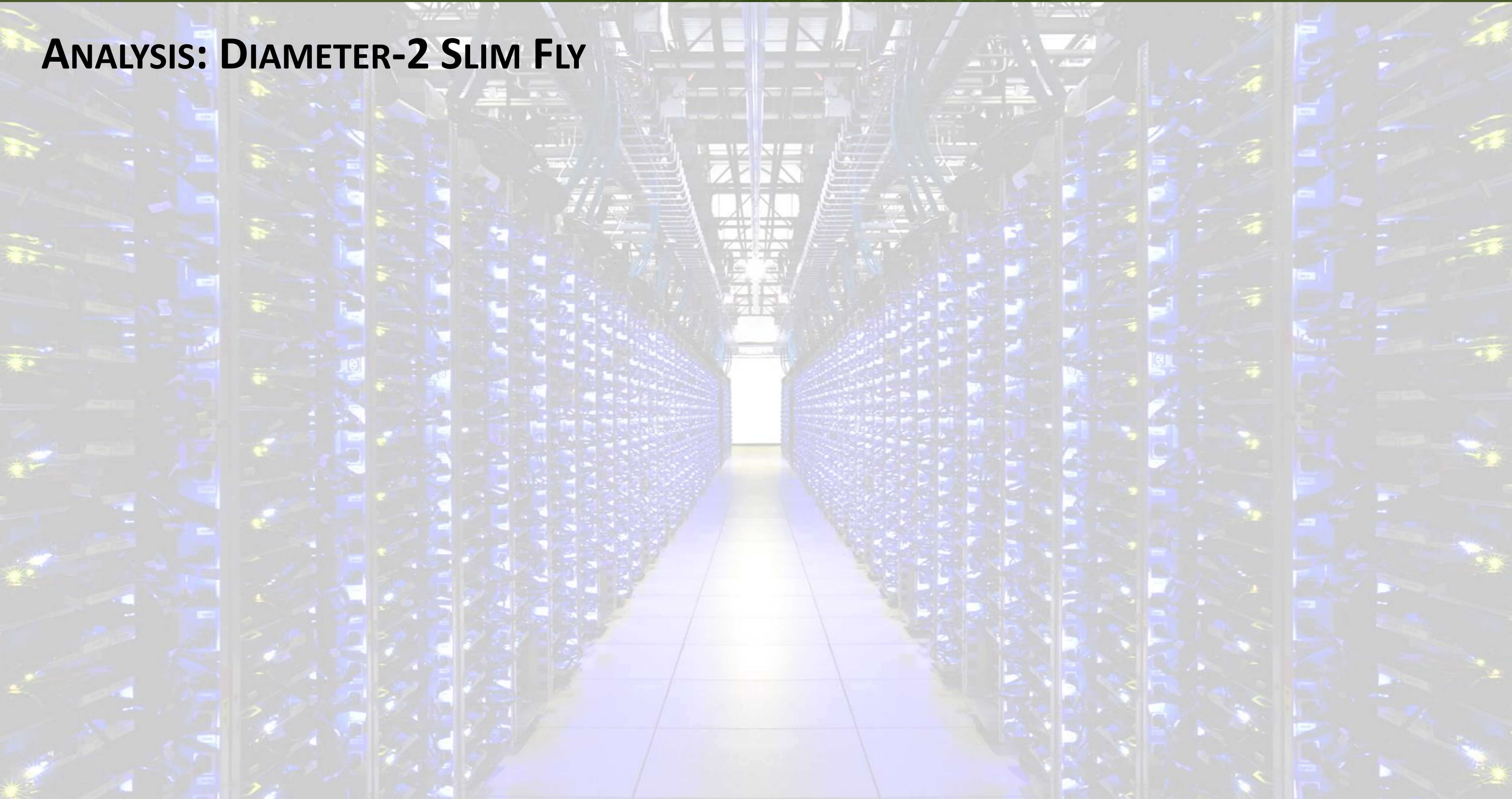
Slim NoC: A Low-Diameter On-Chip Network Topology for High Energy Efficiency and Scalability

Maciej Besta, Syed Minhaj Hassan, Sudhakar Yalamanchili, Rachata Ausavarungnirun, Onur Mutlu, Torsten Hoefler

Analysis: Diameter-2 Slim Fly



Analysis: Diameter-2 Slim Fly

- Lowest latency
- Better throughput than Dragonfly
- Almost-the-best throughput

ANALYSIS: DIAMETER-2 SLIM FLY

~25-30% cost reduction vs. second-best topology (Dragonfly)

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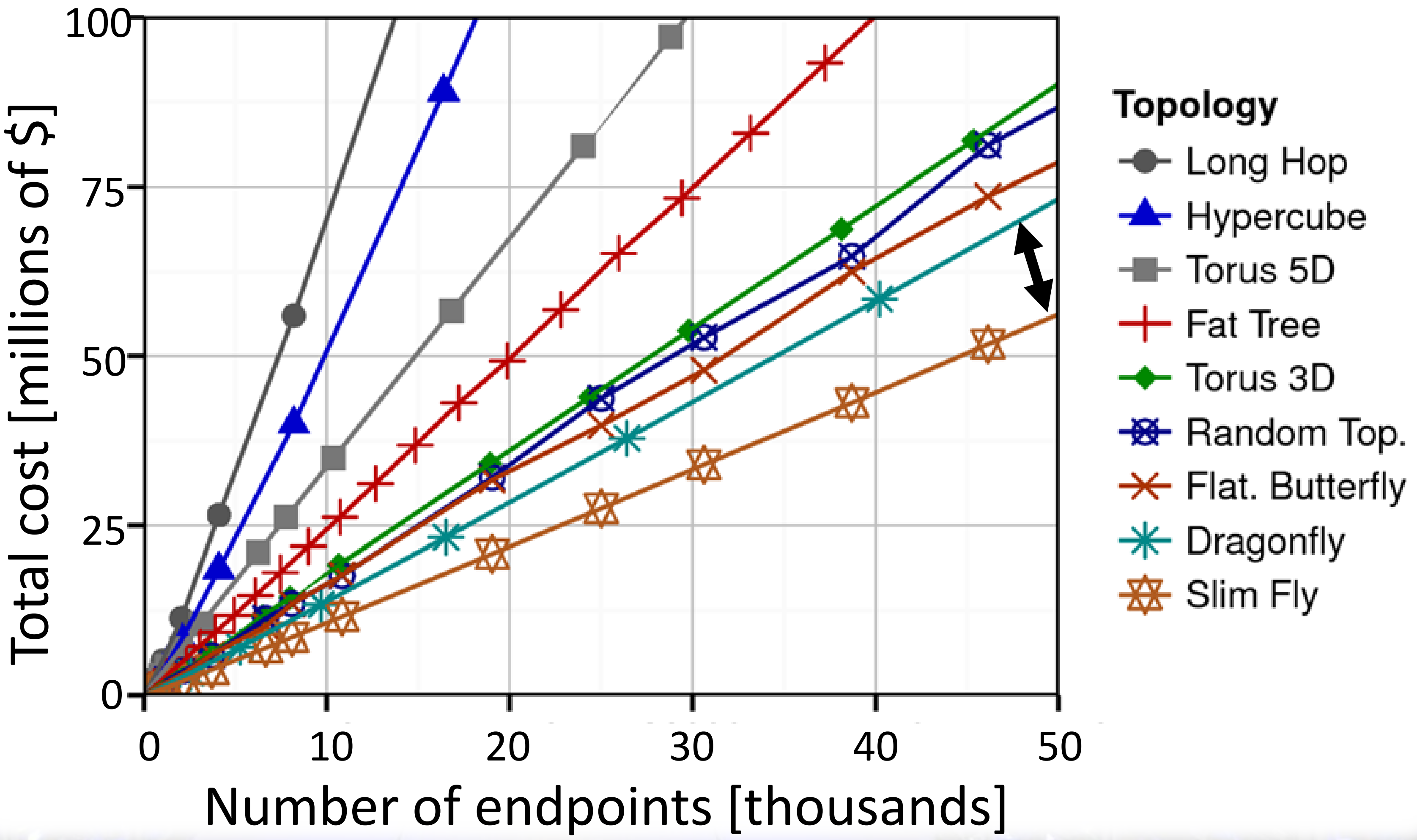
Cost of network construction



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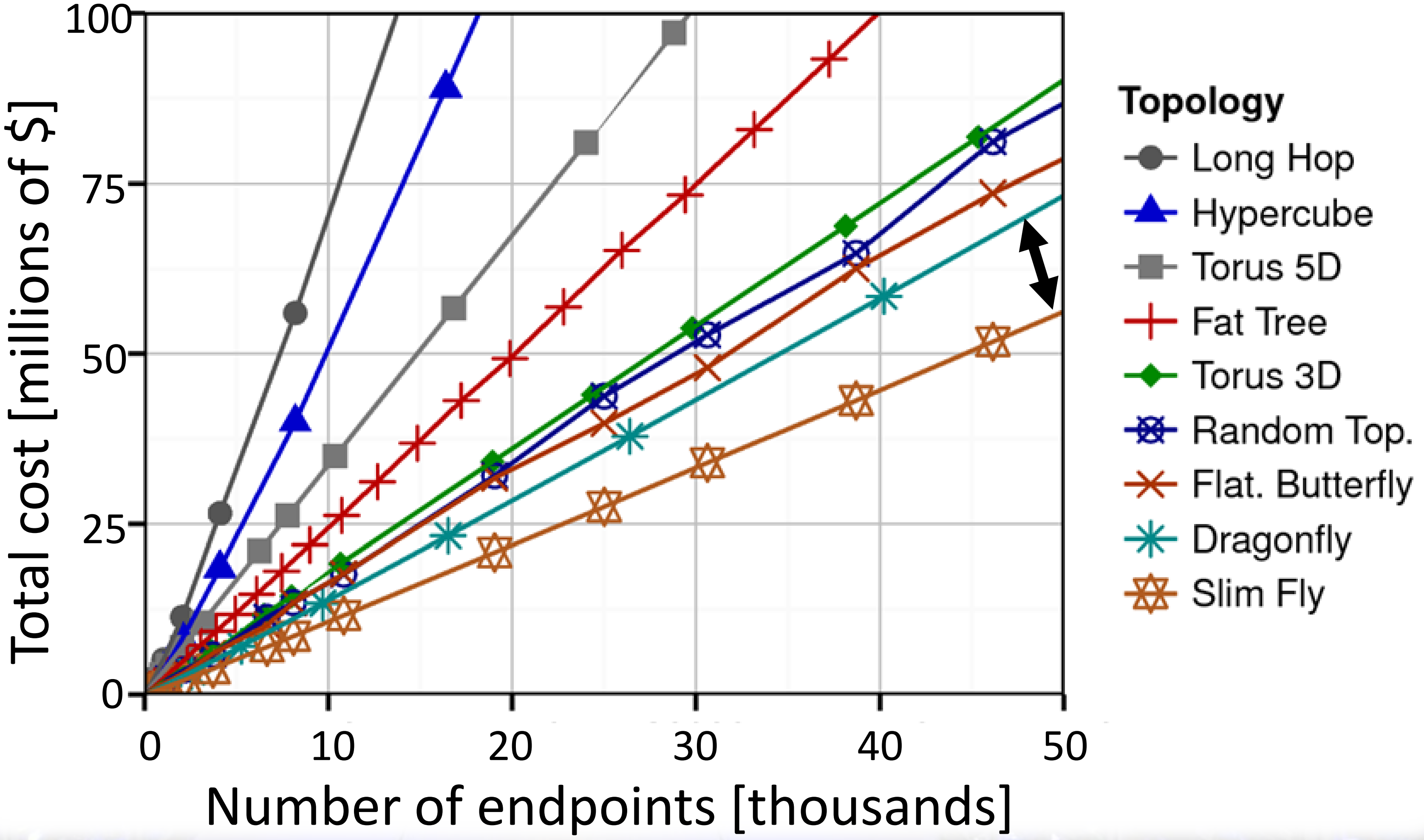

Analysis: Diameter-2 Slim Fly

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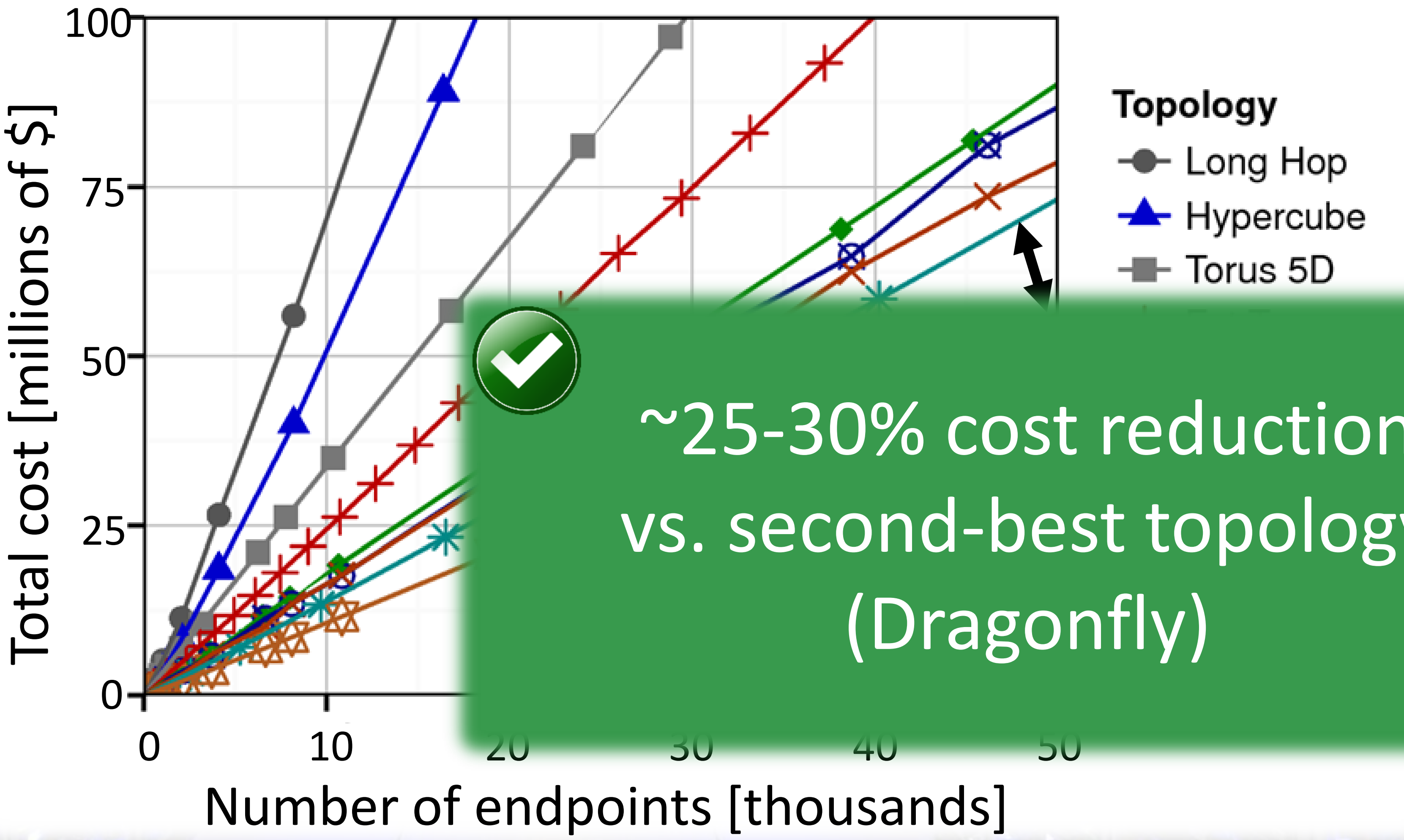

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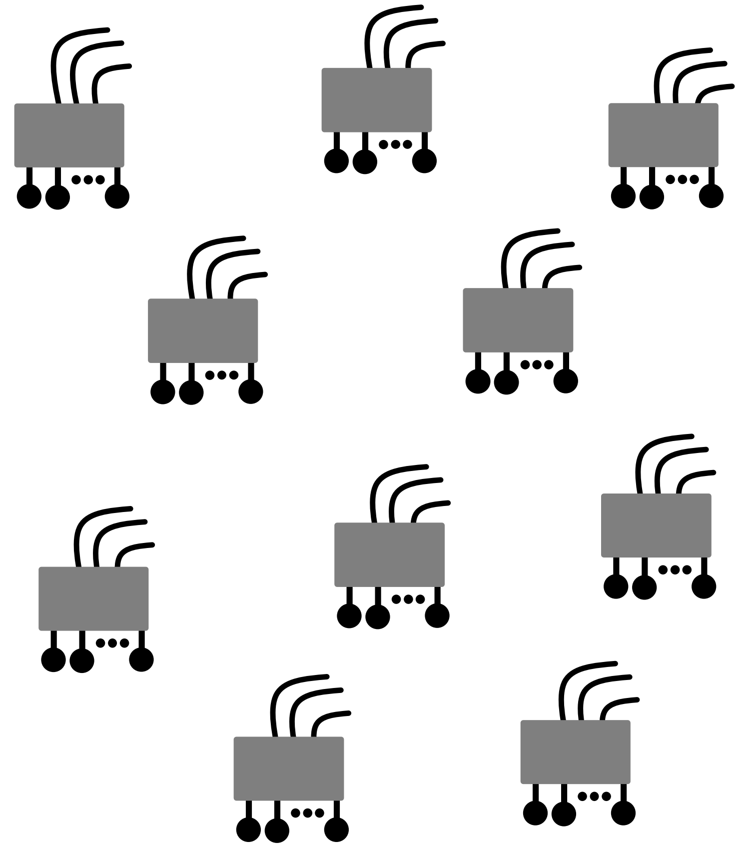
Analysis: Diameter-2 Slim Fly
Performance (Uniform Random)

ANALYSIS: DIAMETER-2 SLIM FLY
PERFORMANCE (UNIFORM RANDOM)



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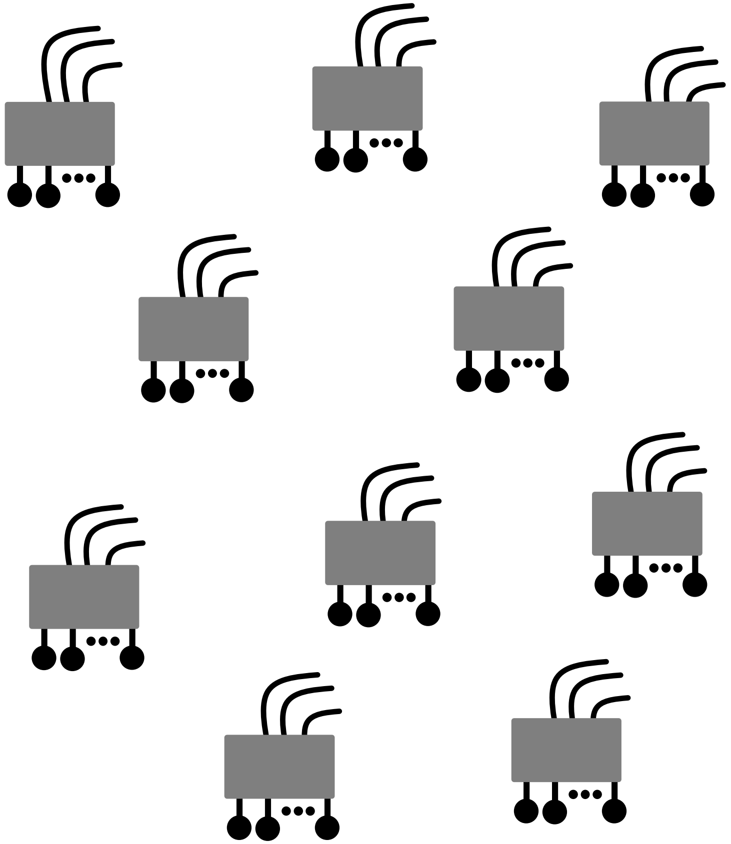

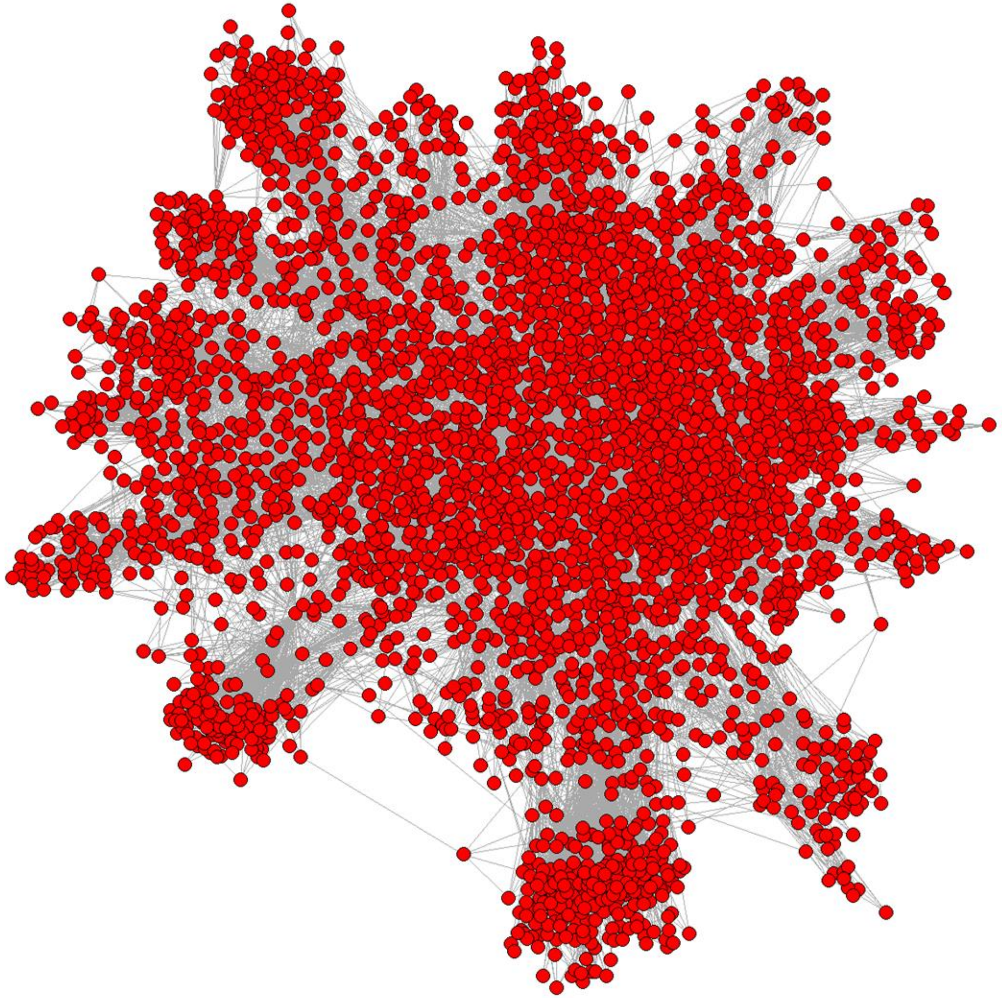

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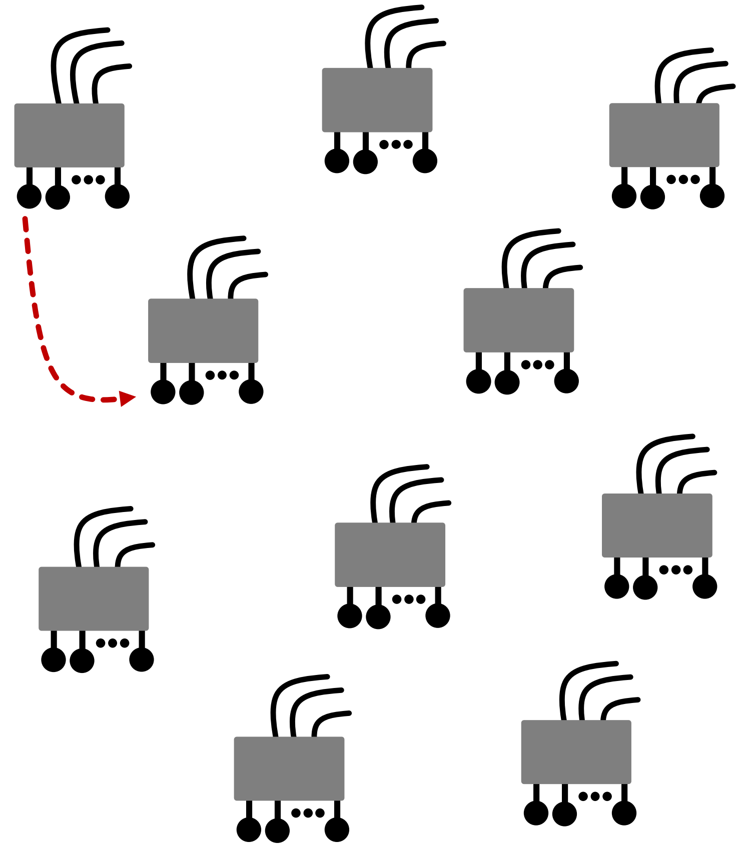

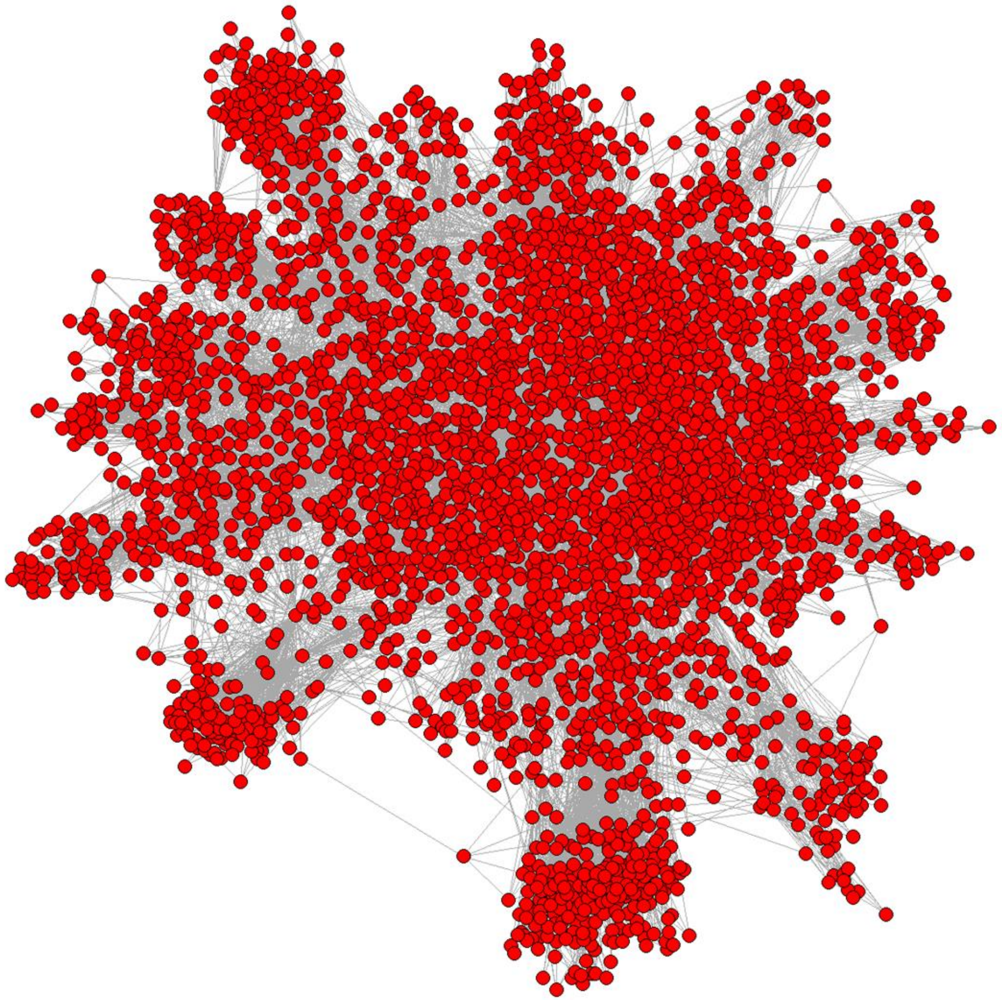

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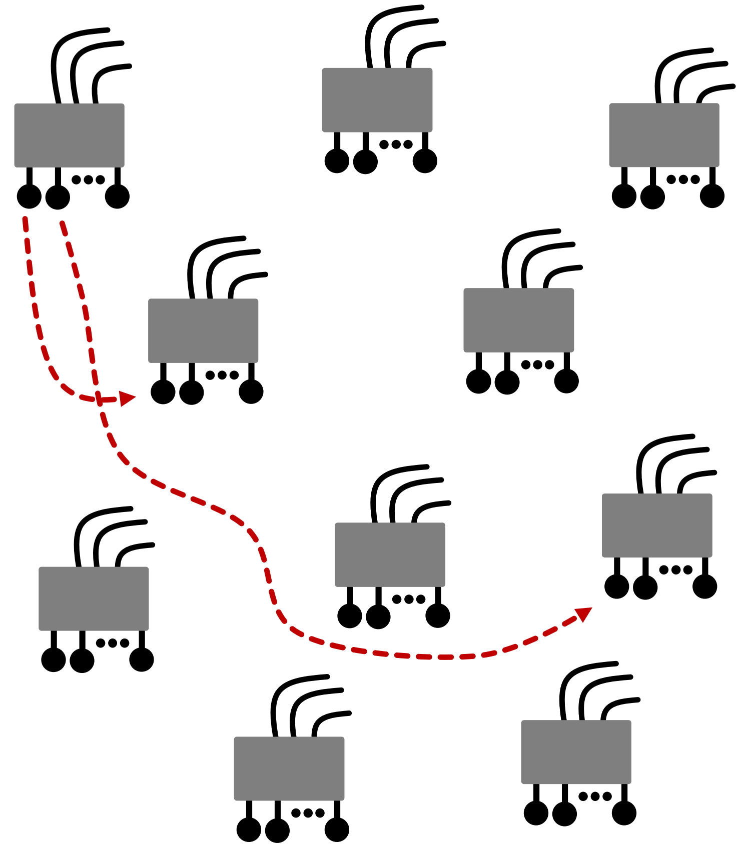

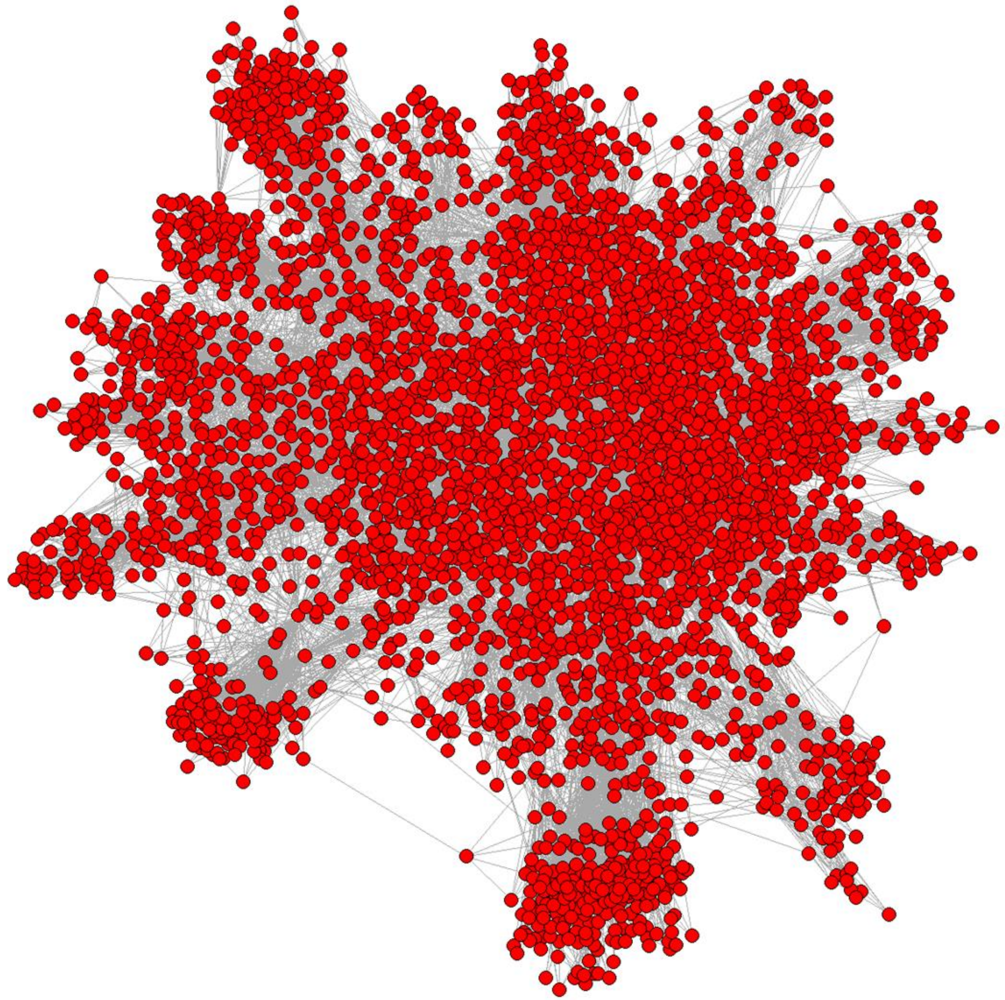

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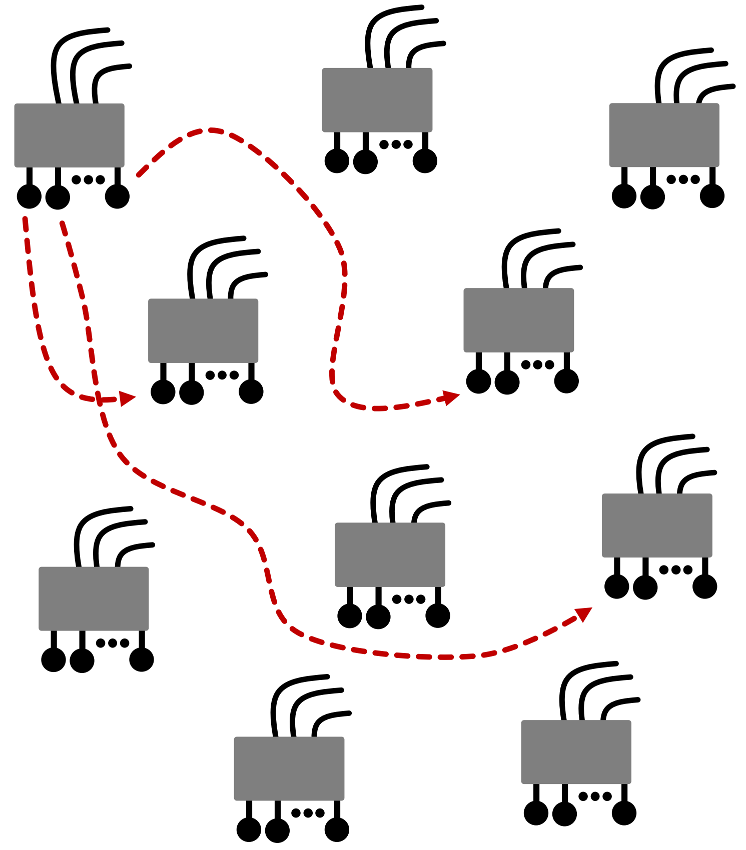

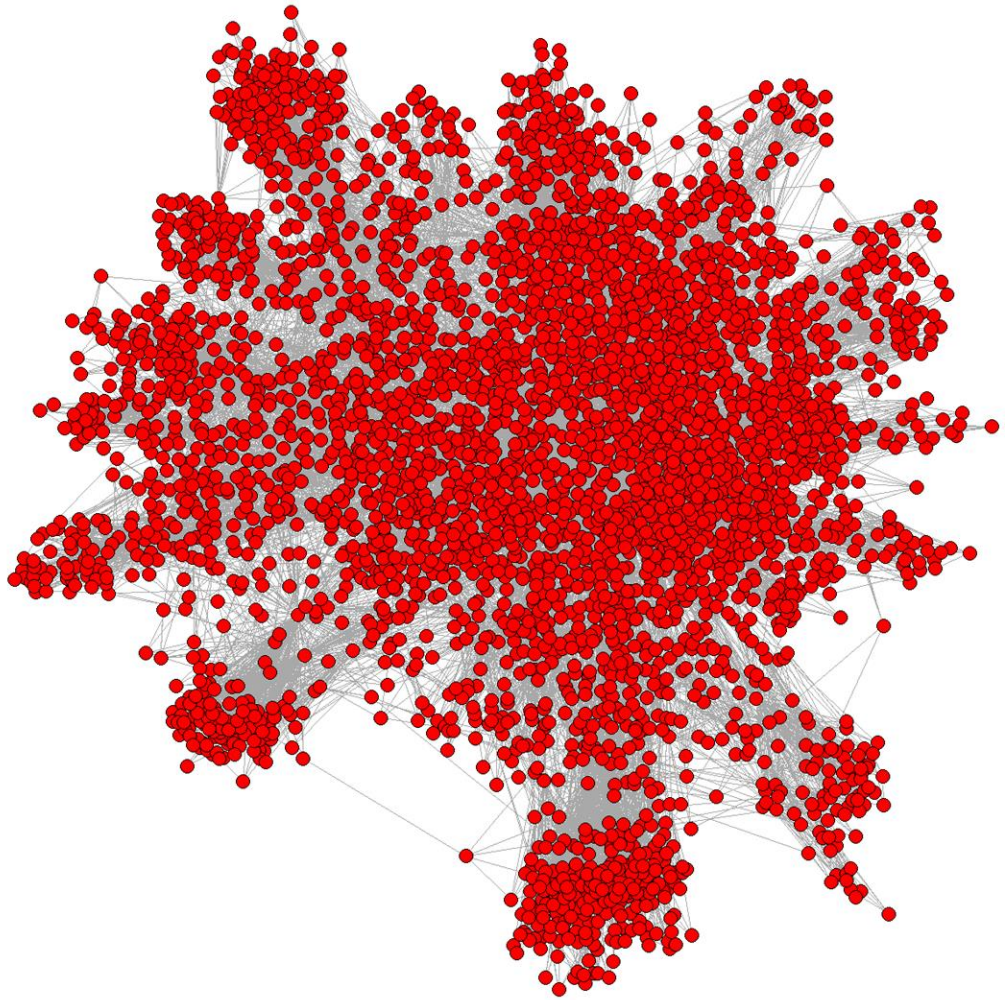

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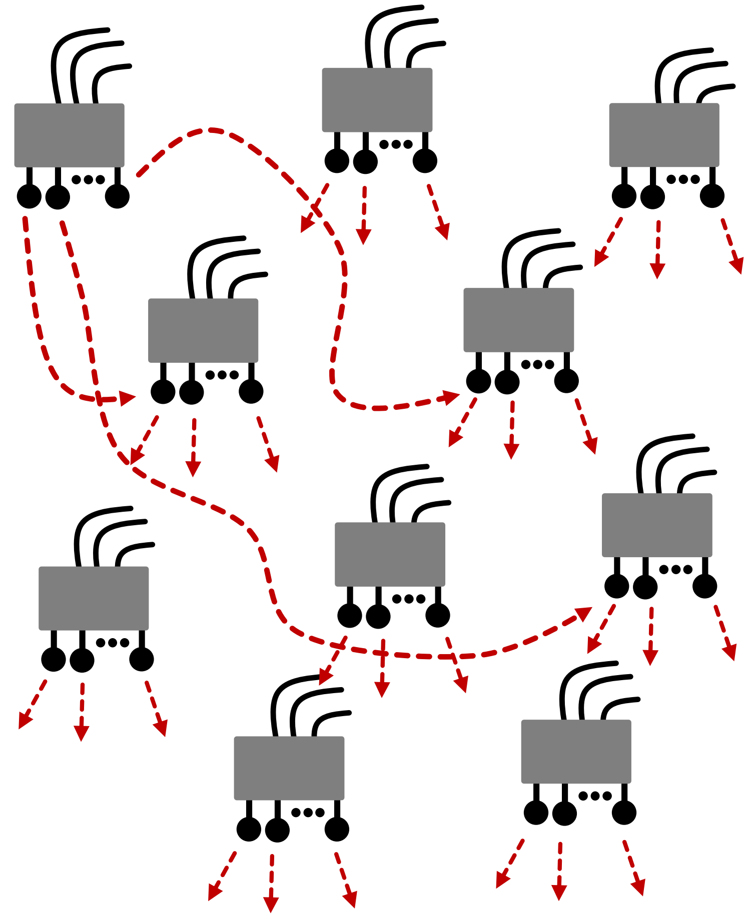

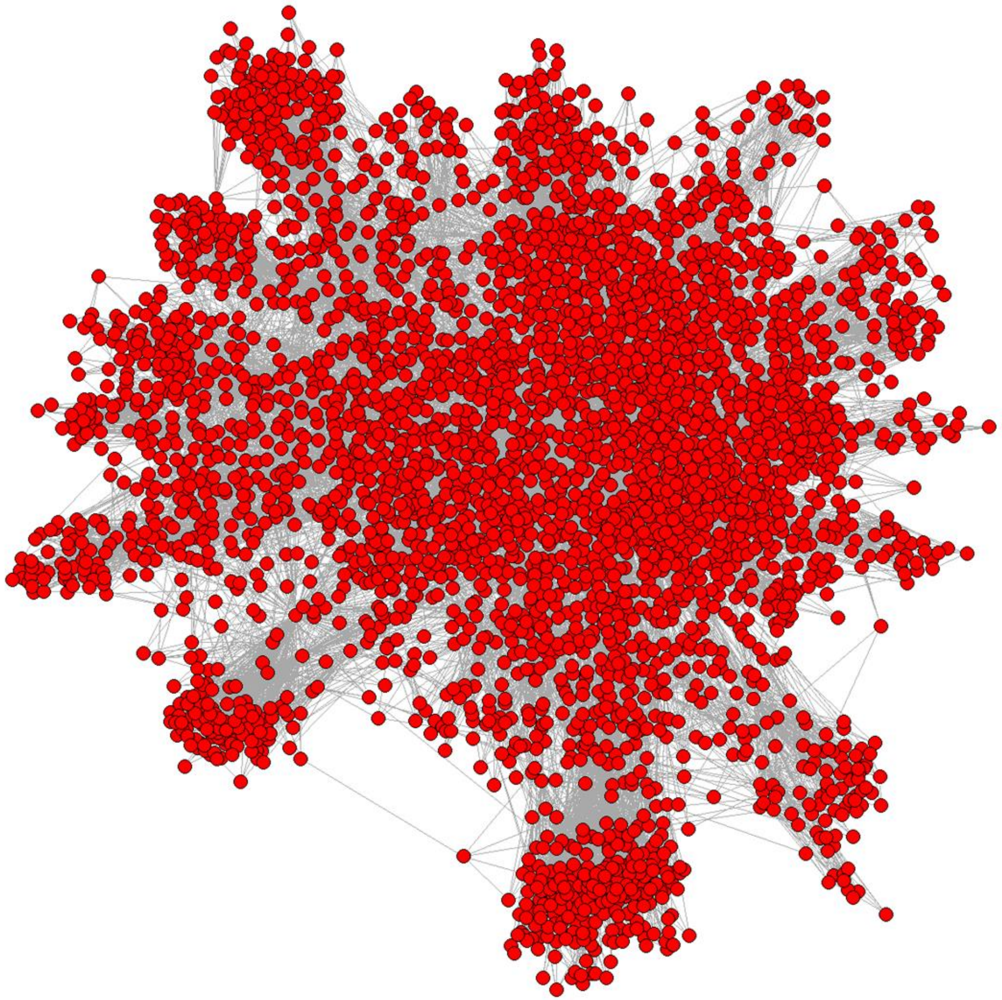

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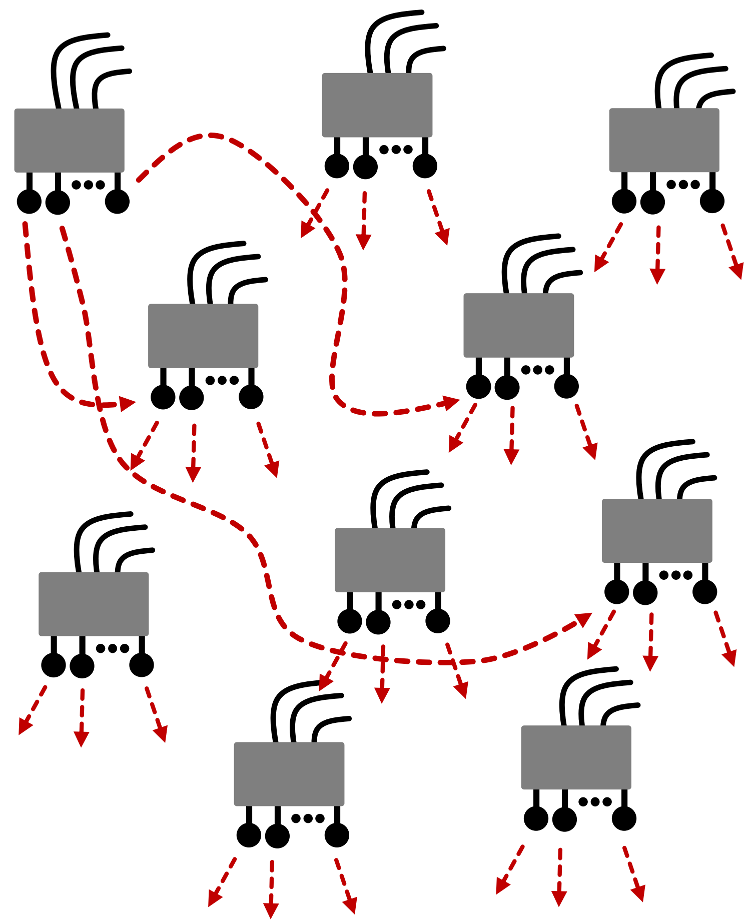

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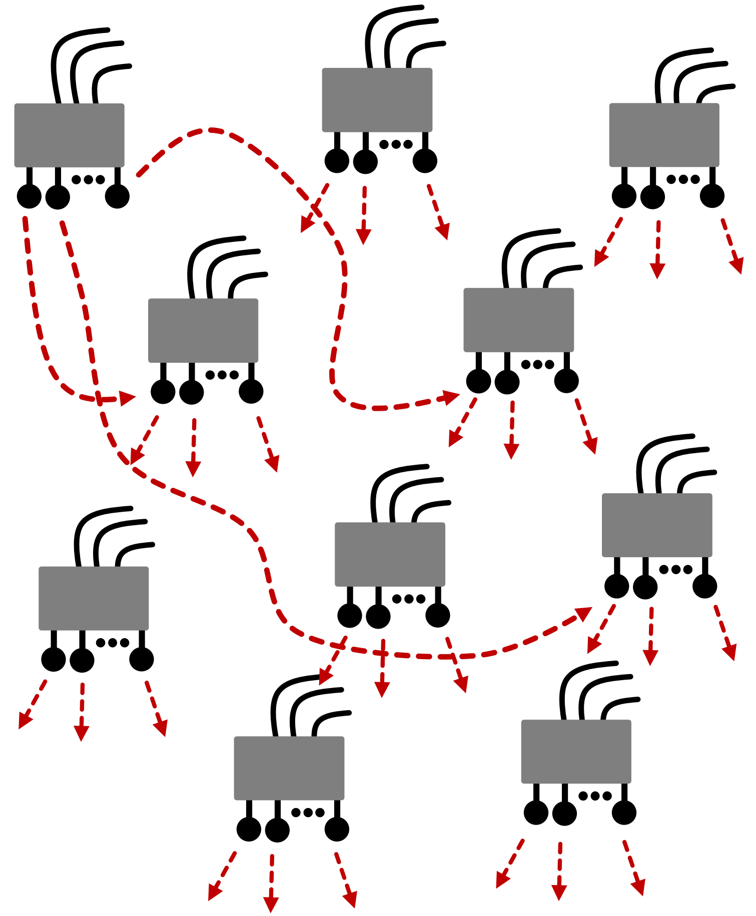
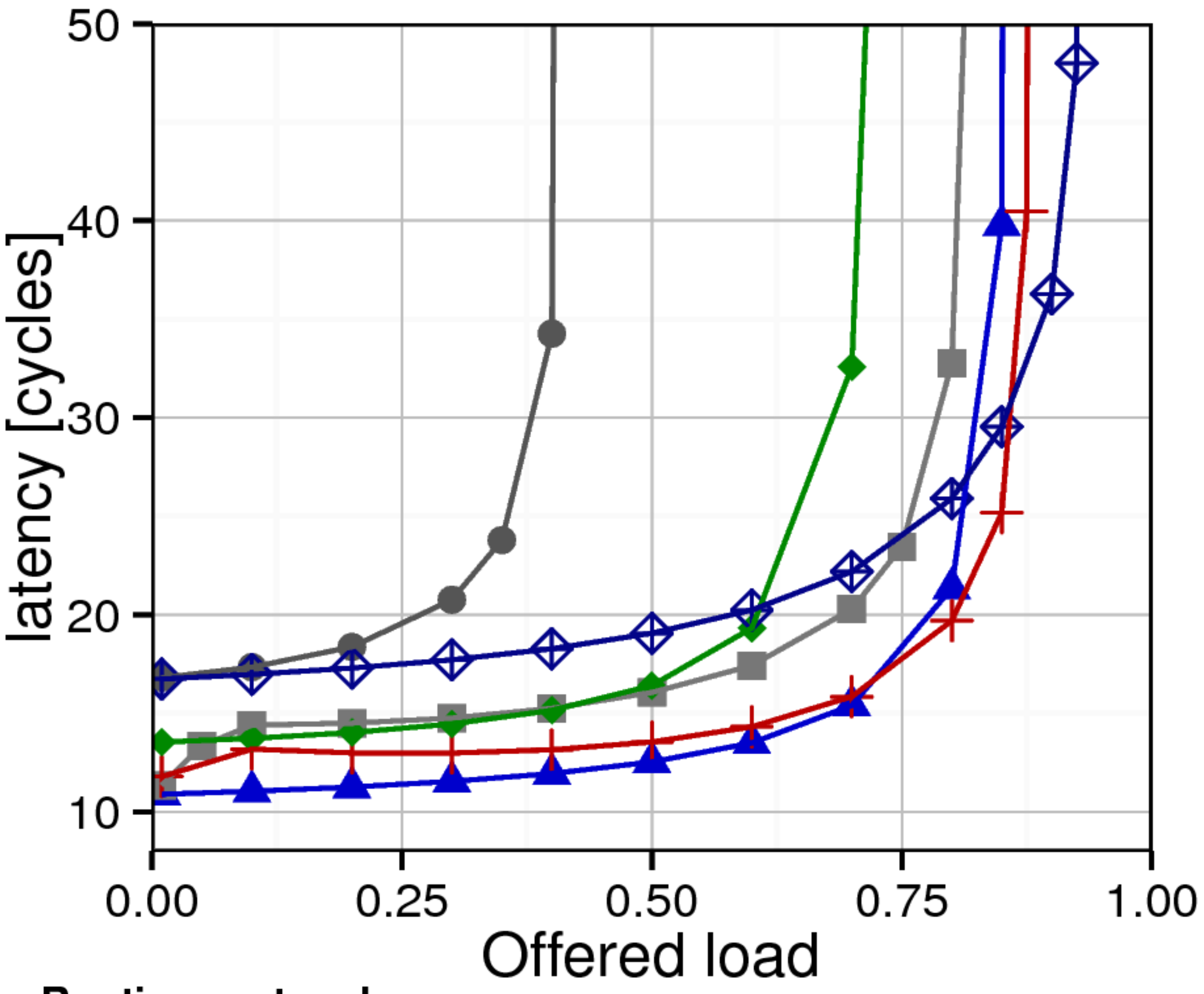
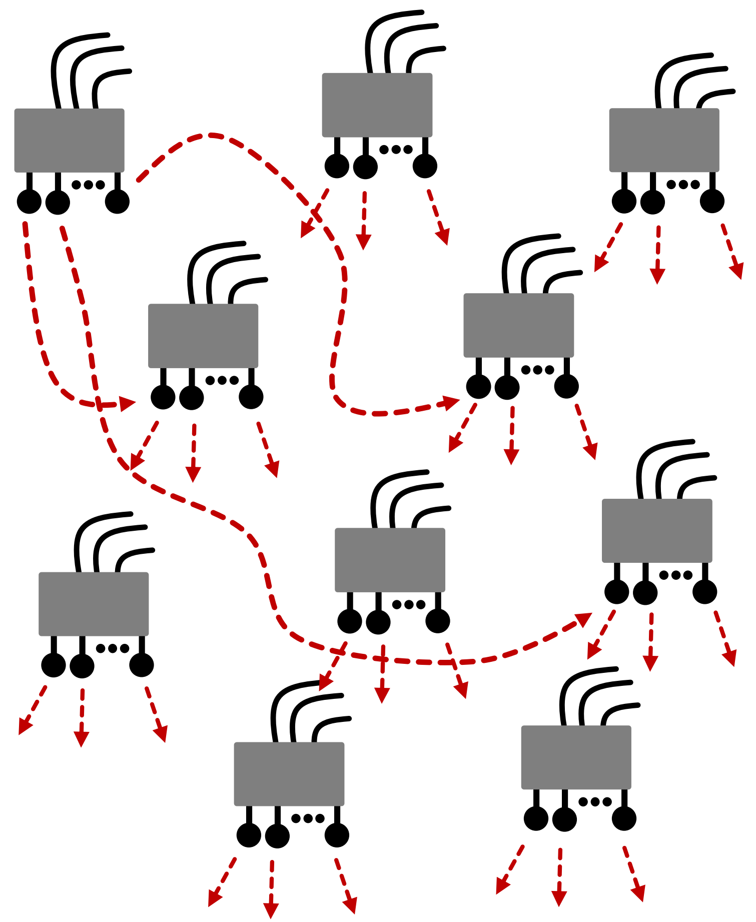
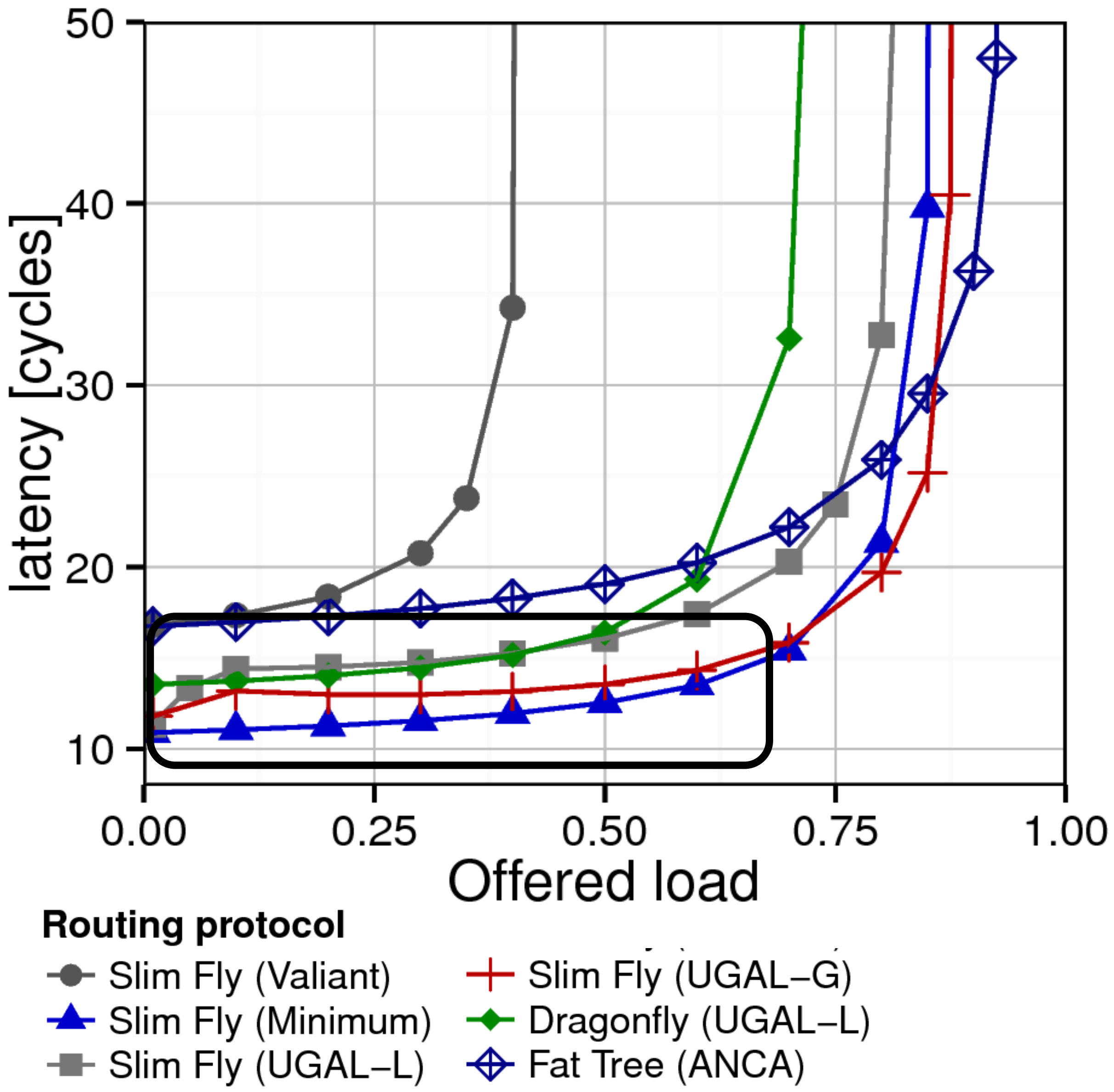




Analysis: Diameter-2 Slim Fly Performance (Uniform Random)





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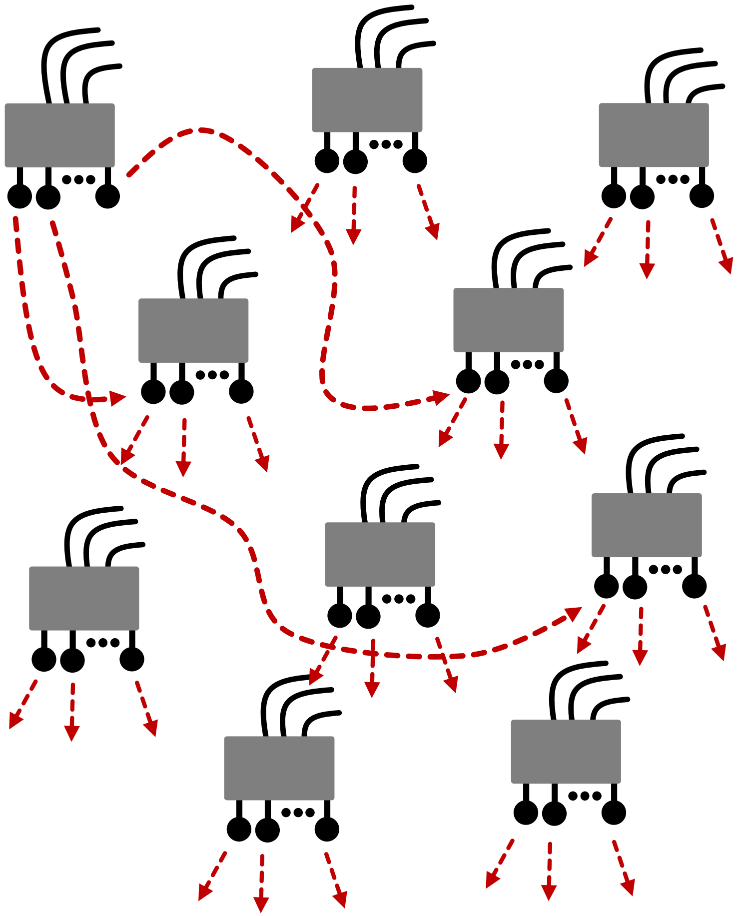

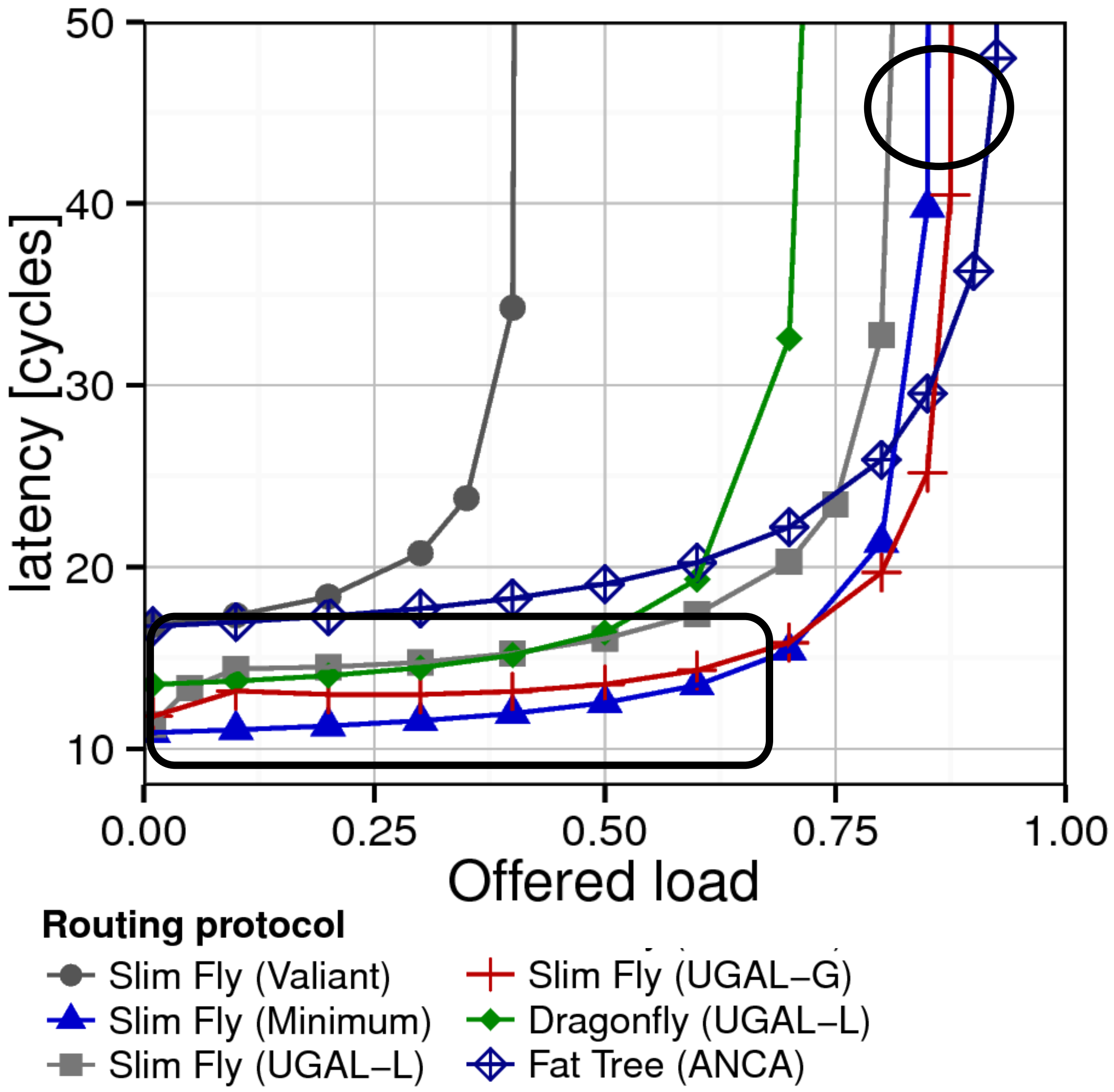

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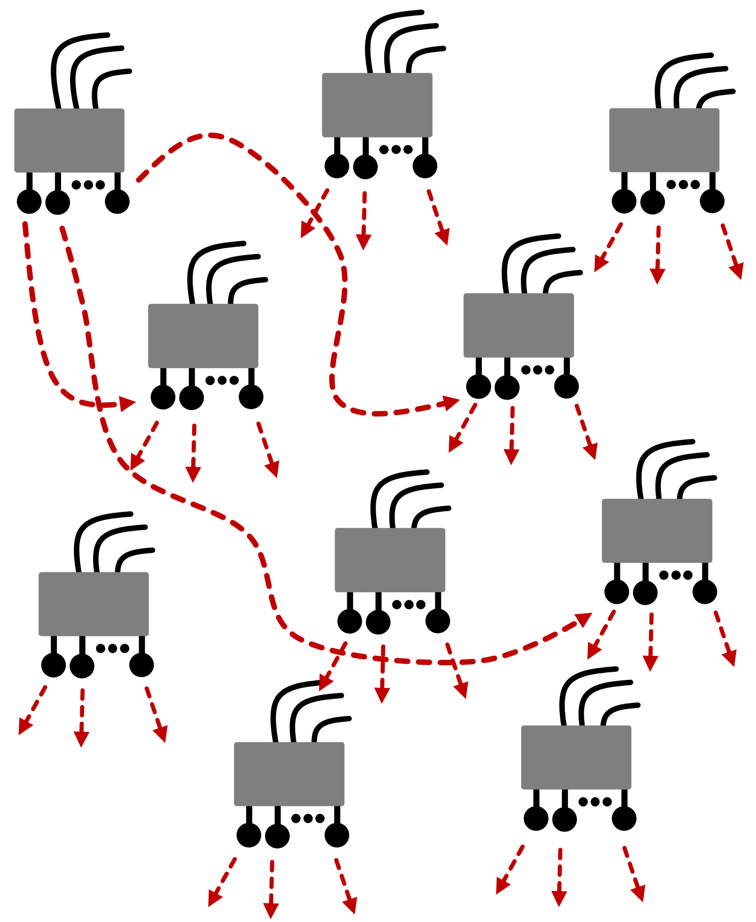

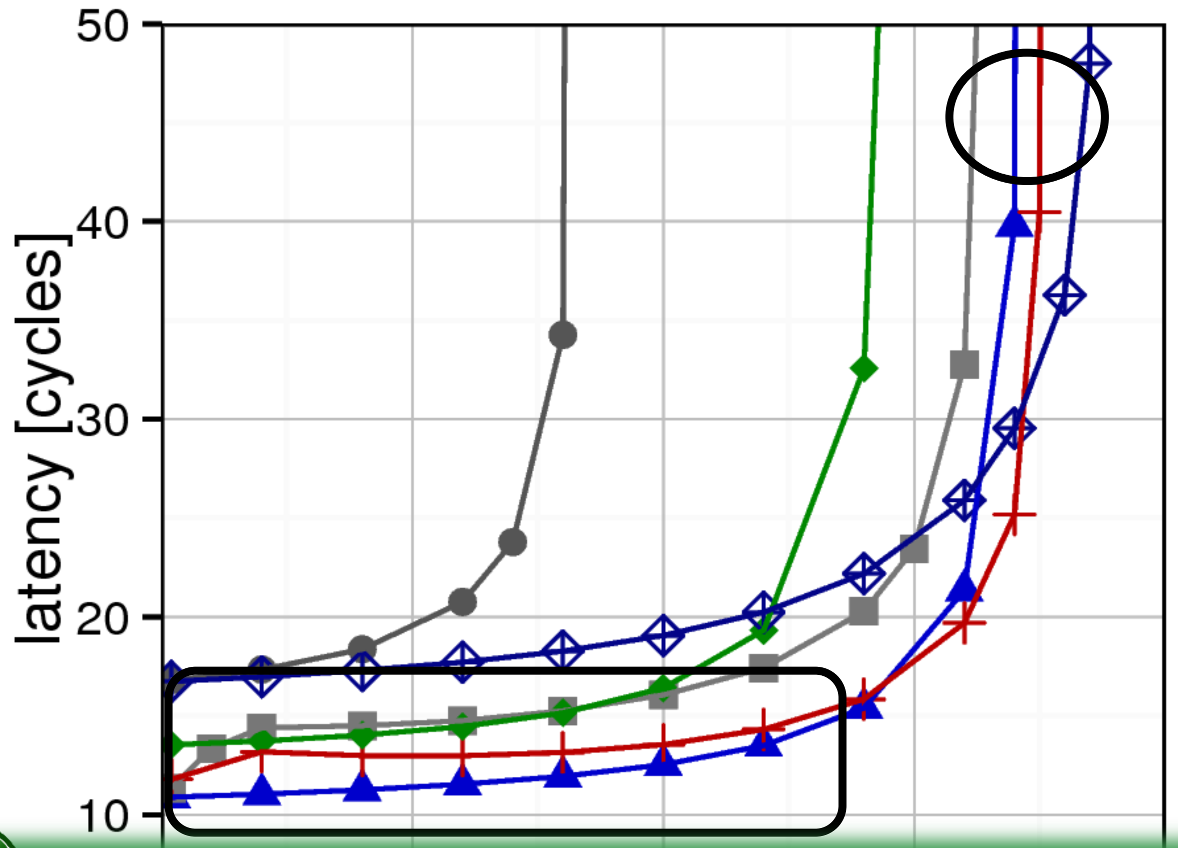

- Lowest latency
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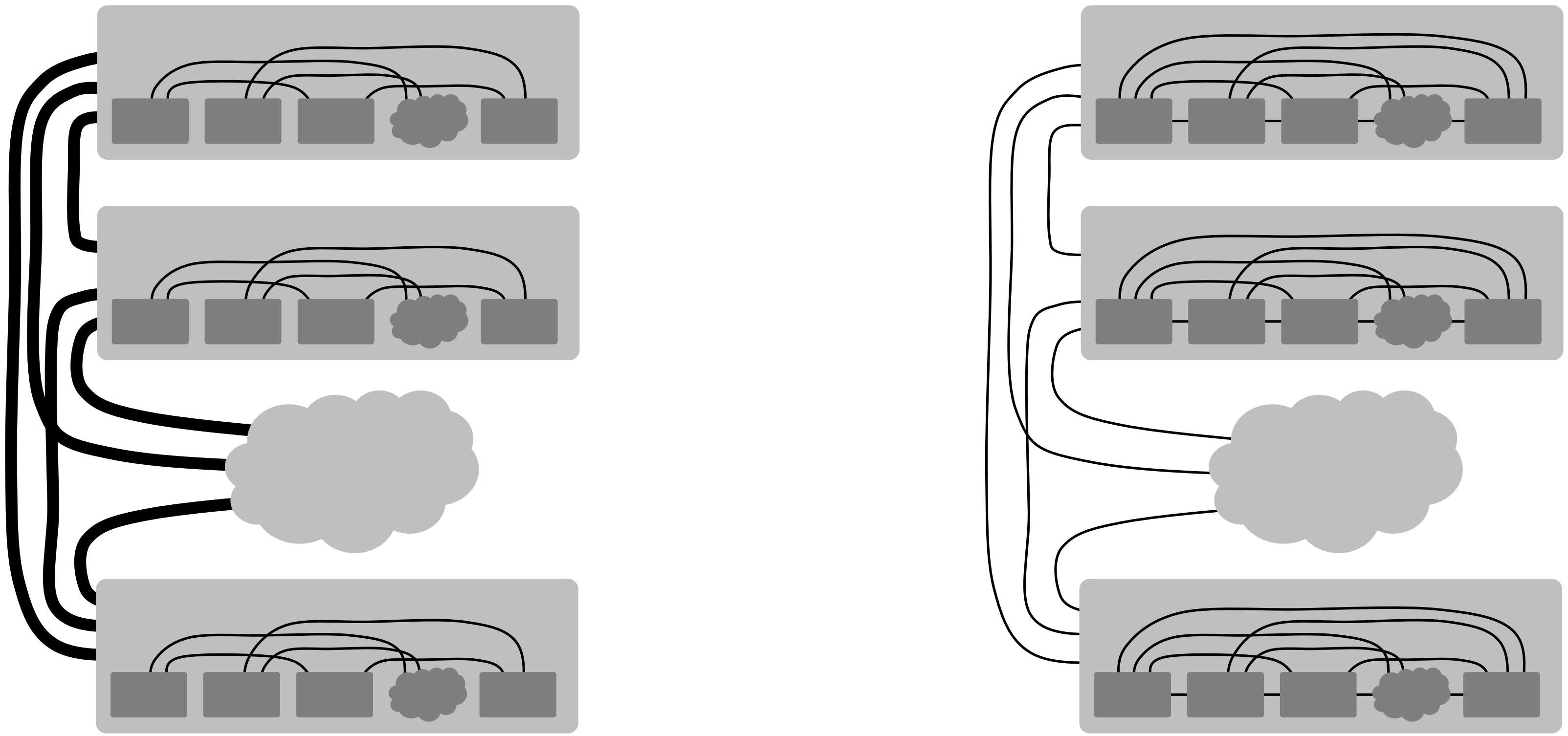
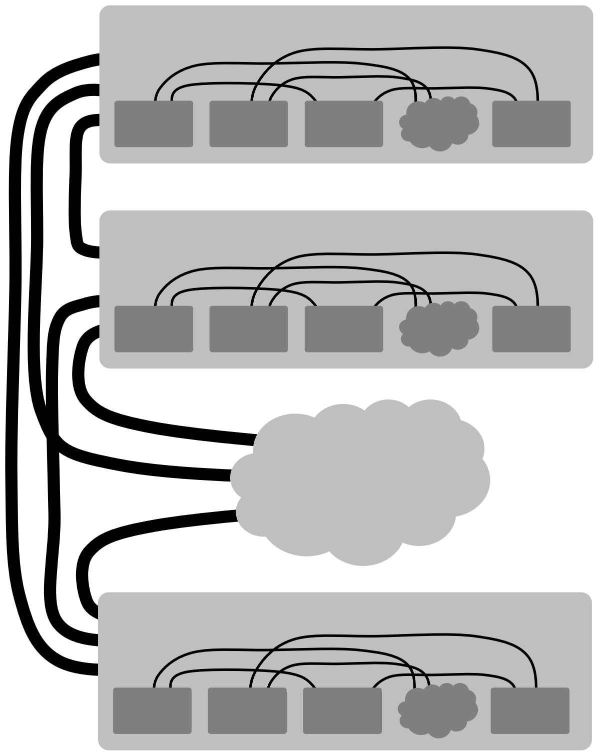
Slim Fly on Chip – First Attempt
Structure Intuition

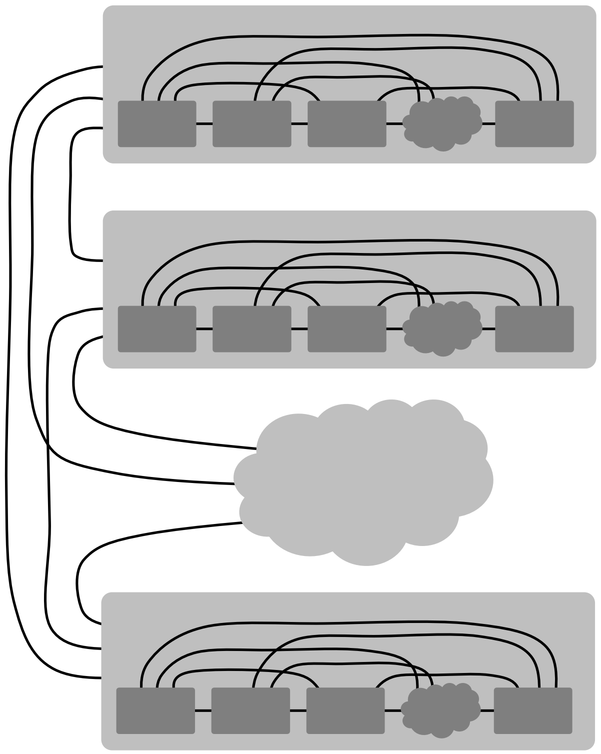


Slim Fly on Chip – First Attempt
Structure Intuition

Slim Fly:



Dragonfly:



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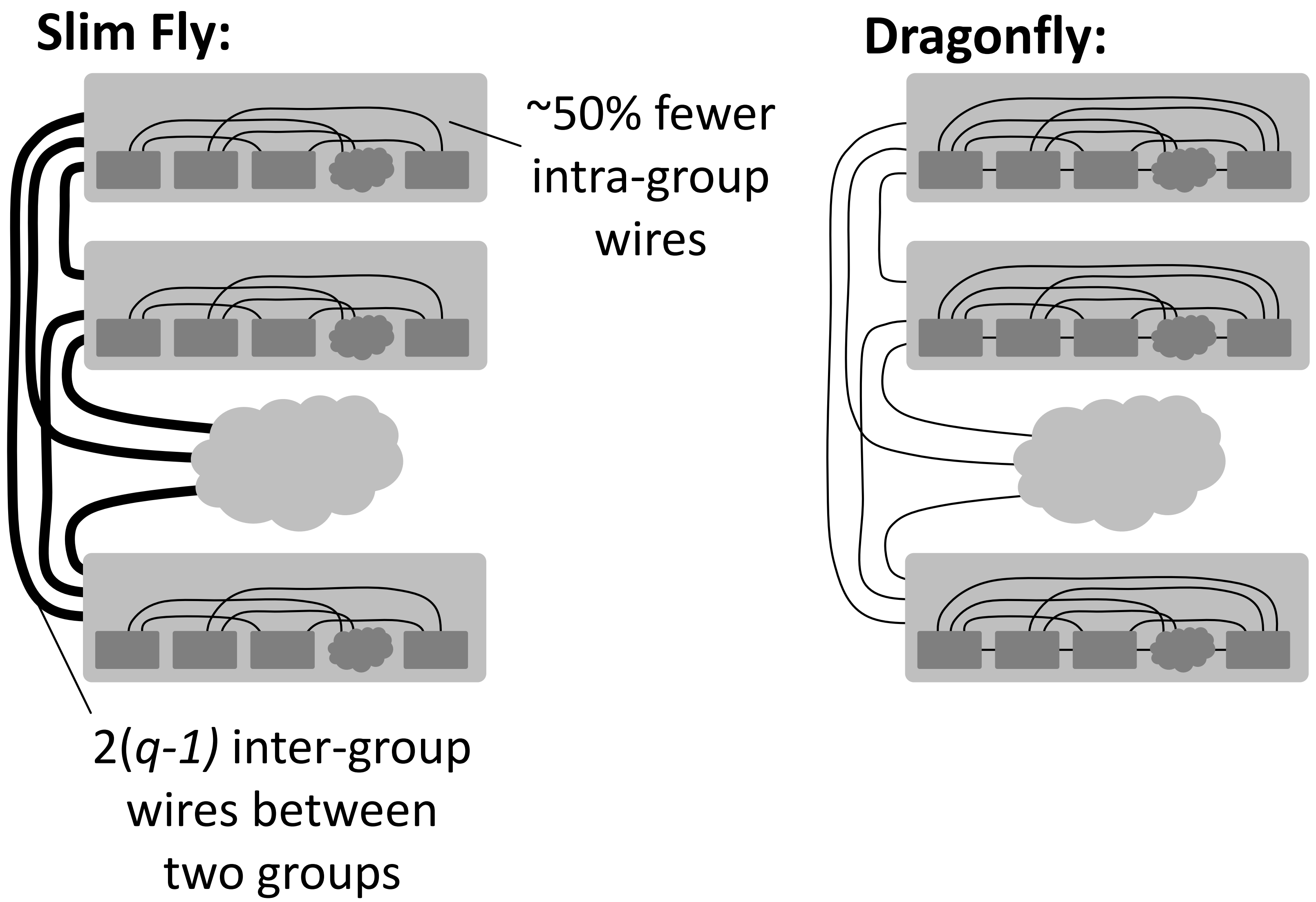
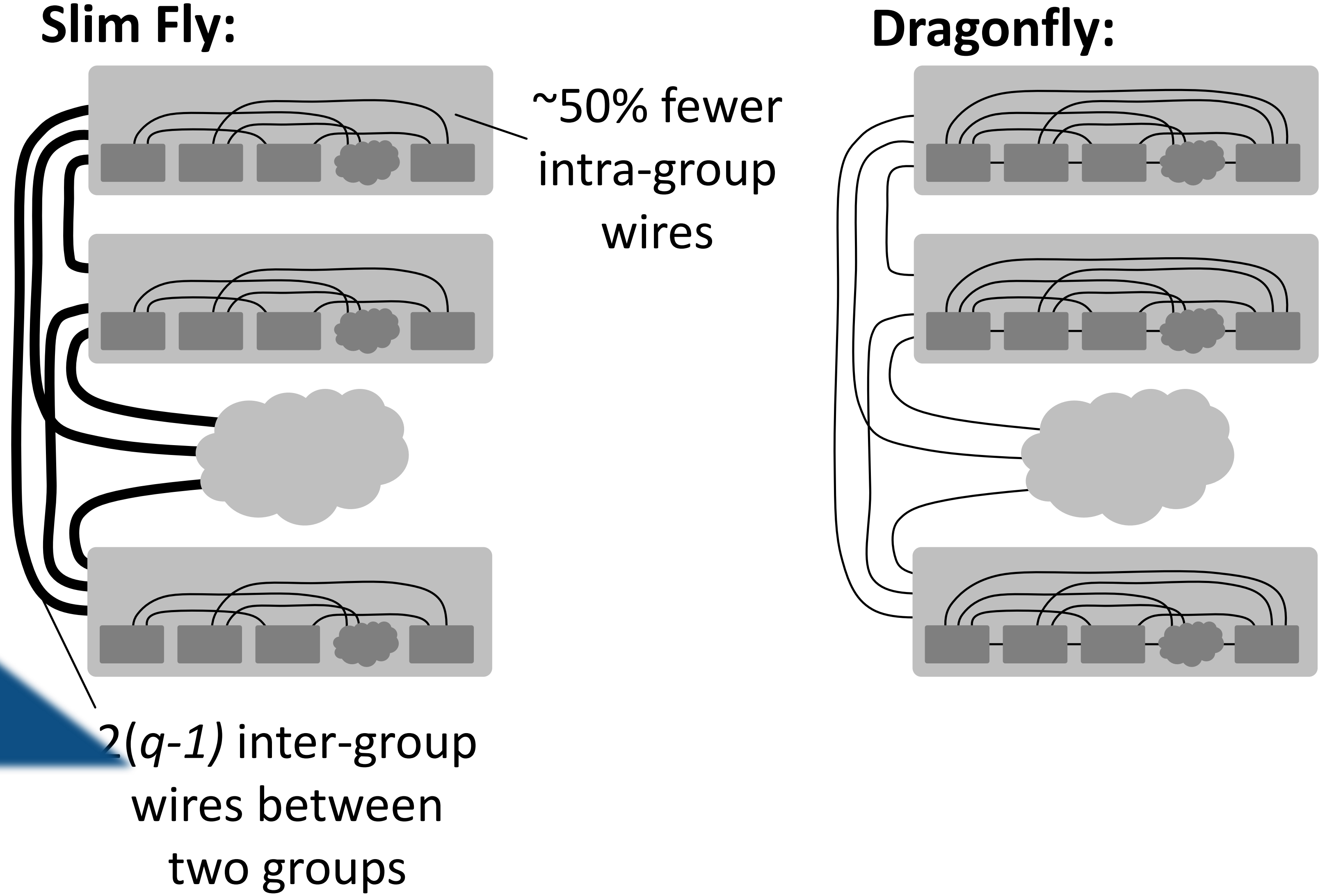
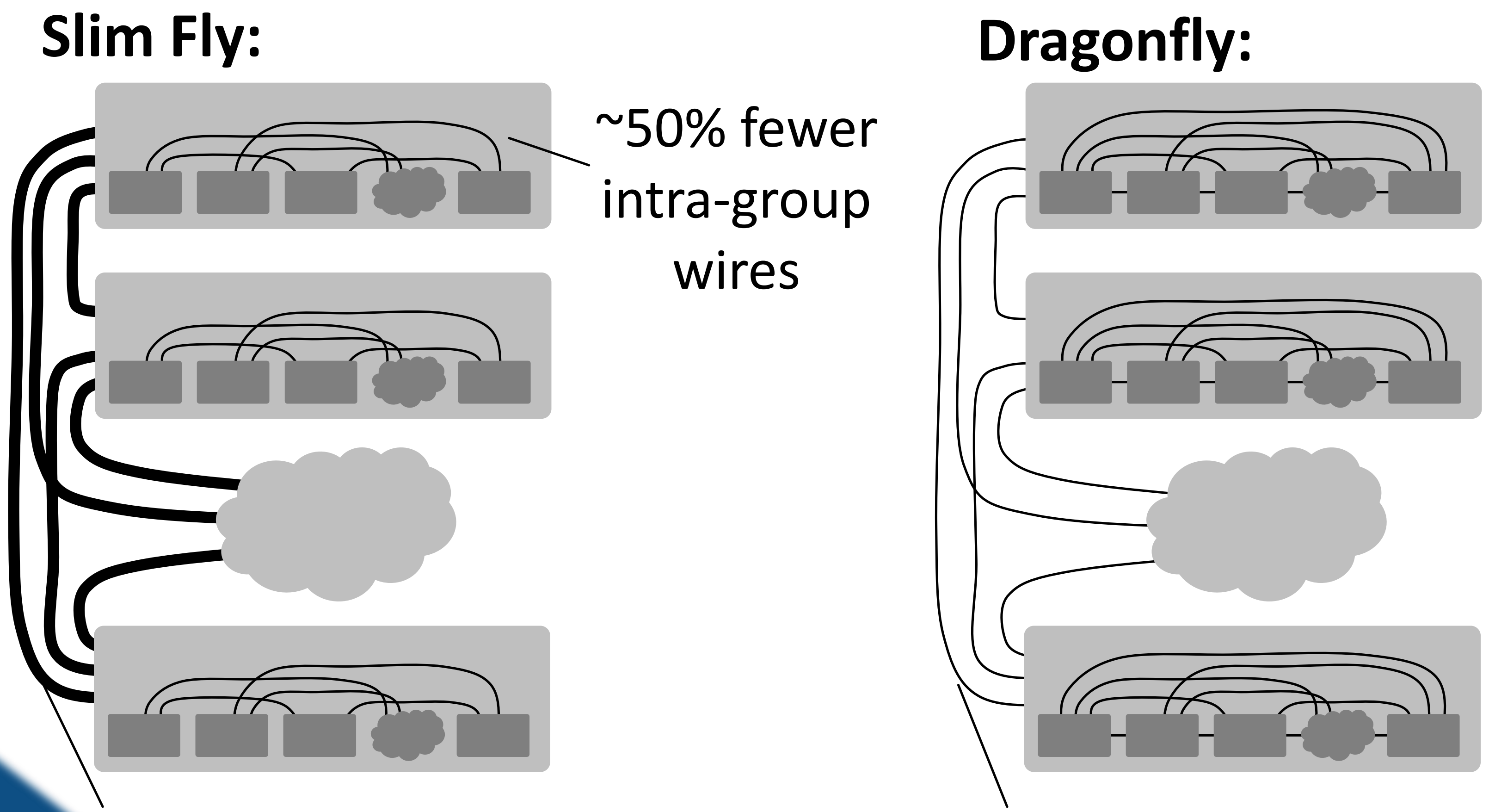


Slim Fly on Chip – First Attempt
Structure Intuition



"*q*": the input parameter that determines the network structure. Formally, the base of a finite field (Slim Fly uses prime *q*; the corresponding field: *{0, 1, …, q-1}*.

Slim Fly on Chip – First Attempt
Structure Intuition



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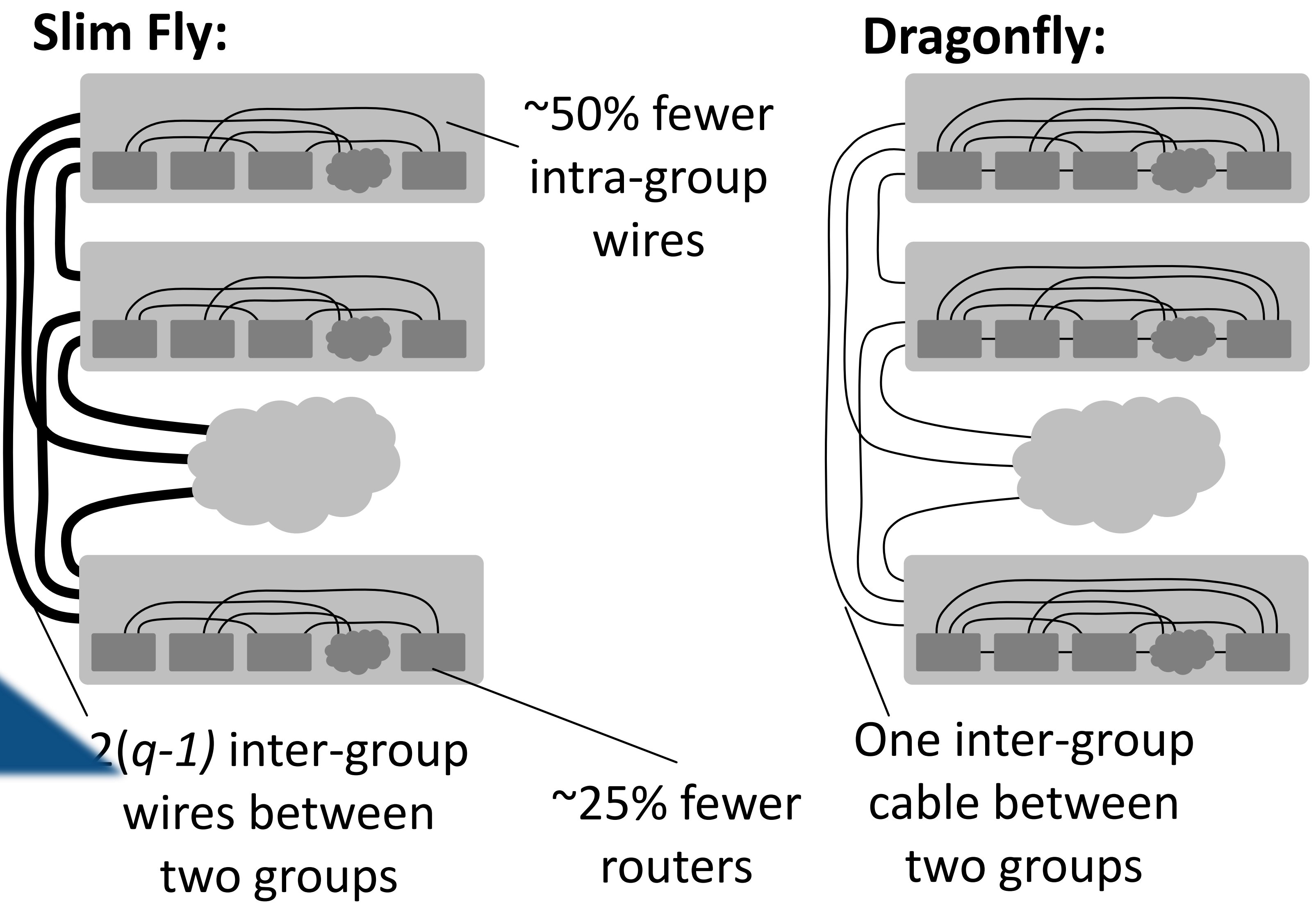
Structure Intuition



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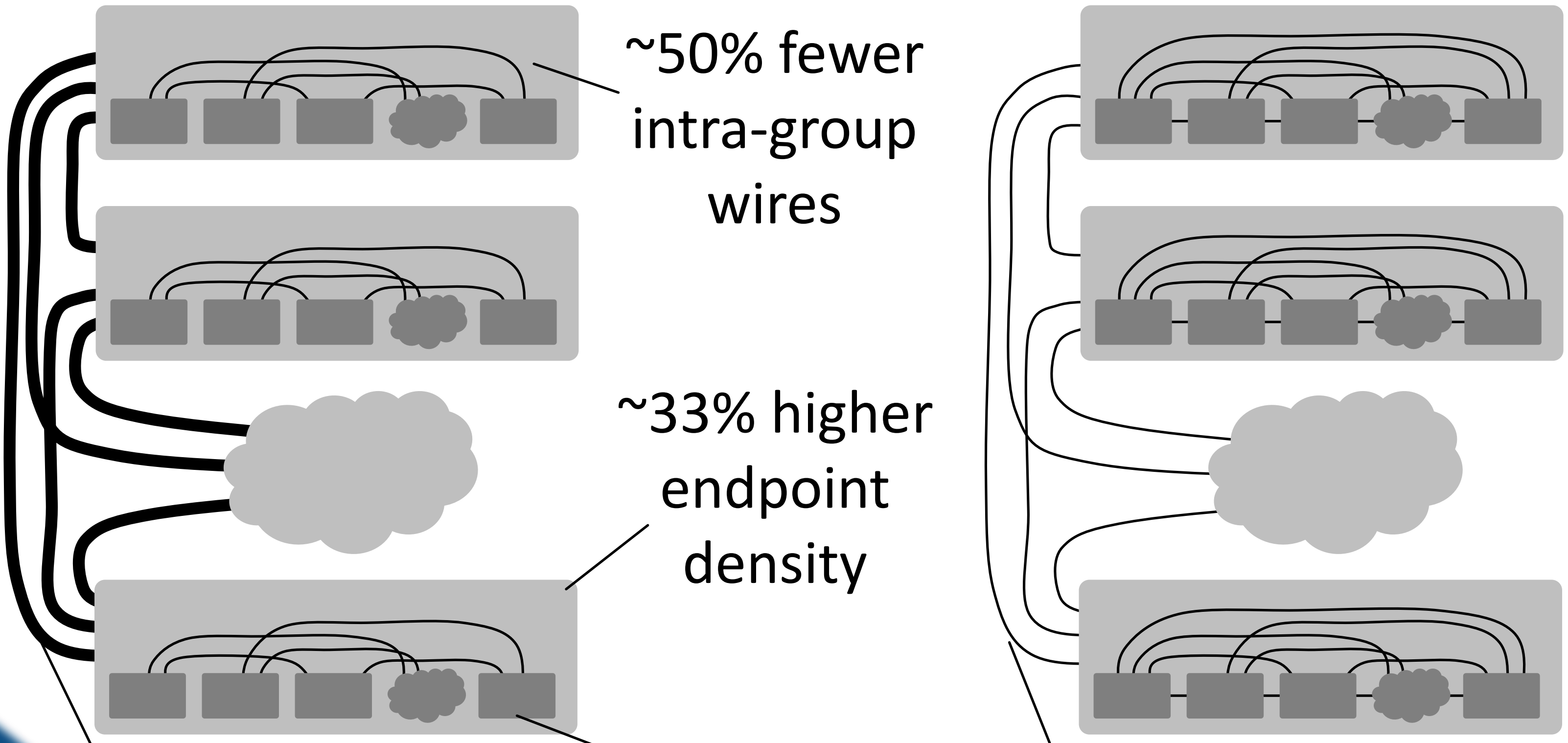
Slim Fly on Chip – First Attempt
Structure Intuition

Slim Fly:

Dragonfly:



~50% fewer intra-group wires

~33% higher endpoint density

2(*q*-1) inter-group wires between two groups

~25% fewer routers

One inter-group cable between two groups

"*q*": the input parameter that determines the network structure. Formally, the base of a finite field (Slim Fly uses prime *q*; the corresponding field: *{0, 1, ..., q-1}*.

Solution: Slim NoC

New cost and area models, new layouts

Let us see some layouts

What difference do they make for lengths of wires?

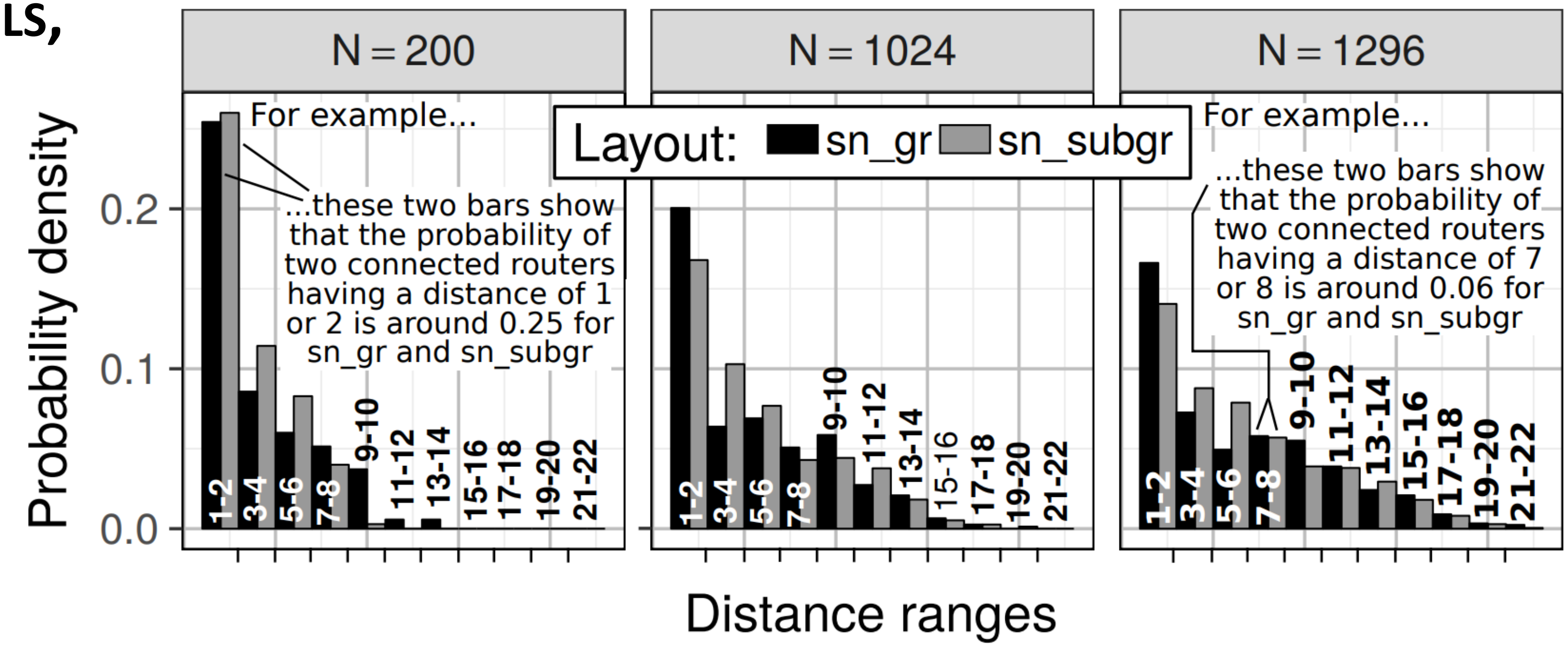
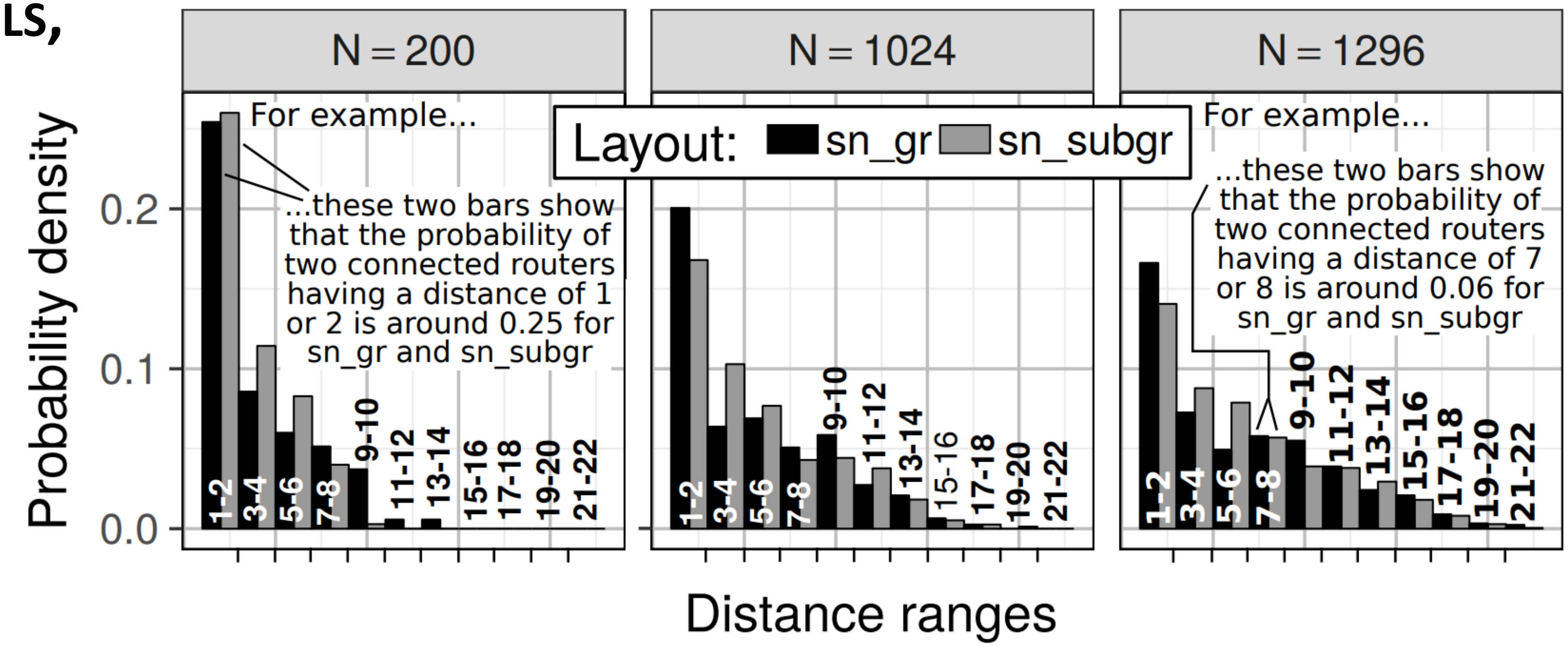


Figure 6. (§ 3.3) Distribution of link distances in SNs. A bar associated with a distance range X illustrates the probability that, for a given layout, two routers are connected with a link that has the distance falling within X. Bars of different colors are placed pairwise so that it is easier to compare the subgroup and group layouts.

Solution: Slim NoC

New cost and area models, new layouts

Let us see some layouts



What difference do they make for lengths of wires?

The "group layout" (sn_gr) is best for 1296 nodes
The "subgroup layout" (sn_subgr) is best for 200 nodes

Solution: Slim NoC
Non-Prime Finite Fields

How to develop such a finite field?

Solution: Slim NoC
Non-Prime Finite Fields

Recap: a finite field $\mathcal{F}_q$

Assuming q is **prime**:

$\mathcal{F}_q = \mathbb{Z}/q\mathbb{Z}$

$= \{0,1, \dots, q-1\}$

(with modular arithmetic).

How to develop such a finite field?

Solution: Slim NoC
Non-Prime Finite Fields

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Example: $q = 5$

50 routers

$\mathcal{F}_5 = \{0,1,2,3,4\}$

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Assuming q is **non-prime**:

$\mathcal{F}_q = \mathbb{Z}/q\mathbb{Z} = \{x_0, x_1, \ldots, x_{q-1}\}$

...with instruction tables that define operations on the field.

Solution: Slim NoC
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How to develop such a finite field?

Example: $q = 9$

162 routers

$\mathcal{F}_9 = \{0,1,2,u,v,w,x,y,z\}$

Solution: Slim NoC
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162 routers

$\mathcal{F}_9 = \{0,1,2,u,v,w,x,y,z\}$

+	0	1	2	u	v	w	x	y	z
0	0	1	2	u	v	w	x	y	z
1	1	2	0	v	w	u	y	z	x
2	2	0	1	w	u	v	z	x	y
u	u	v	w	x	y	z	0	1	2
v	v	w	u	y	z	x	1	2	0
w	w	u	v	z	x	y	2	0	1
x	x	y	z	0	1	2	u	v	w
y	y	z	x	1	2	0	v	w	u
z	z	x	y	2	0	1	w	u	v

Addition

SOLUTION: SLIM NOC
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0	0	1	2	u	v	w	x	y	z
1	1	2	0	v	w	u	y	z	x
2	2	0	1	w	u	v	z	x	y
u	u	v	w	x	y	z	0	1	2
v	v	w	u	y	z	x	1	2	0
w	w	u	v	z	x	y	2	0	1
x	x	y	z	0	1	2	u	v	w
y	y	z	x	1	2	0	v	w	u
z	z	x	y	2	0	1	w	u	v

Addition

×	0	1	2	u	v	w	x	y	z
0	0	0	0	0	0	0	0	0	0
1	0	1	2	u	v	w	x	y	z
2	0	2	1	x	z	y	u	w	v
u	0	u	x	2	w	z	1	v	y
v	0	v	z	w	x	1	y	2	u
w	0	w	y	z	1	u	v	x	2
x	0	x	u	1	y	v	2	z	w
y	0	y	w	v	2	x	z	u	1
z	0	z	v	y	u	2	w	1	x

Multiplication

Solution: Slim NoC
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1	1	2	0	v	w	u	y	z	x
2	2	0	1	w	u	v	z	x	y
u	u	v	w	x	y	z	0	1	2
v	v	w	u	y	z	x	1	2	0
w	w	u	v	z	x	y	2	0	1
x	x	y	z	0	1	2	u	v	w
y	y	z	x	1	2	0	v	w	u
z	z	x	y	2	0	1	w	u	v

Addition

×	0	1	2	u	v	w	x	y	z
0	0	0	0	0	0	0	0	0	0
1	0	1	2	u	v	w	x	y	z
2	0	2	1	x	z	y	u	w	v
u	0	u	x	2	w	z	1	v	y
v	0	v	z	w	x	1	y	2	u
w	0	w	y	z	1	u	v	x	2
x	0	x	u	1	y	v	2	z	w
y	0	y	w	v	2	x	z	u	1
z	0	z	v	y	u	2	w	1	x

Multiplication

elem	−*elem*
0	0
1	2
2	0
u	x
v	z
w	y
x	u
y	w
z	v

Inverse

SOLUTION: SLIM NOC
NON-PRIME FINITE FIELDS

Recap: a finite field $\mathcal{F}_q$

Assuming q is **prime**:

$\mathcal{F}$

$=$

(v

arithmetic).

Generate with
an exhaustive search,
or use a construction
based on polynomials

Example: $q = 5$

50 routers

$\mathcal{F}_5 = \{0,1,2,3,4\}$

How to develop such a finite field?

Assuming q is **non-prime**:

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1	1	2	0	v	w	u	y	z	x
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v	v	w	u	y	z	x	1	2	0
w	w	u	v	z	x	y	2	0	1
x	x	y	z	0	1	2	u	v	w
y	y	z	x	1	2	0	v	w	u
z	z	x	y	2	0	1	w	u	v

Addition

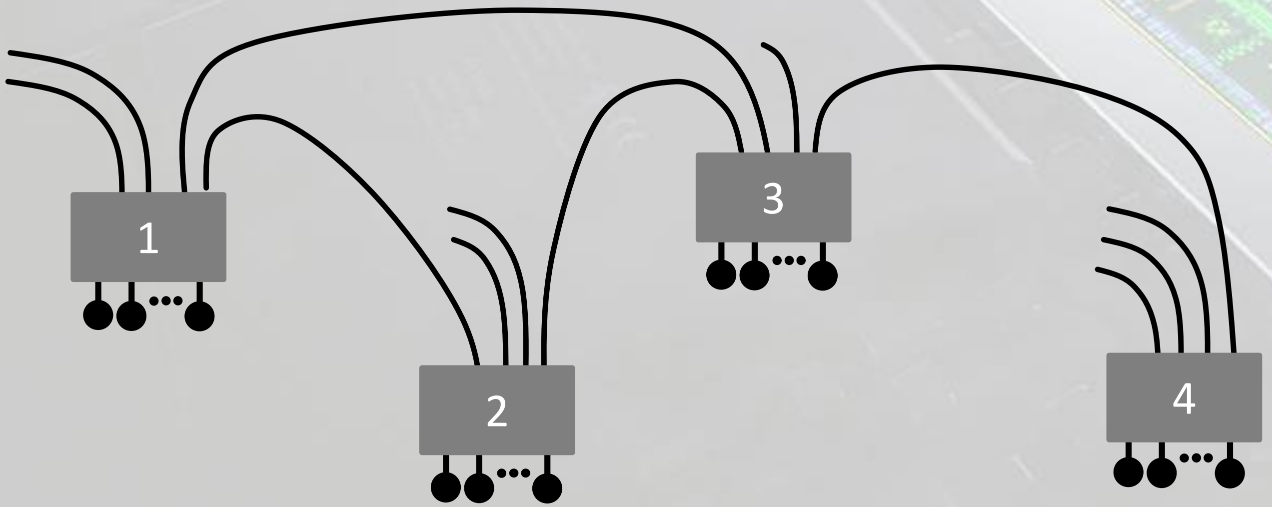
×	0	1	2	u	v	w	x	y	z
0	0	0	0	0	0	0	0	0	0
1	0	1	2	u	v	w	x	y	z
2	0	2	1	x	z	y	u	w	v
u	0	u	x	2	w	z	1	v	y
v	0	v	z	w	x	1	y	2	u
w	0	w	y	z	1	u	v	x	2
x	0	x	u	1	y	v	2	z	w
y	0	y	w	v	2	x	z	u	1
z	0	z	v	y	u	2	w	1	x

Multiplication

elem	−*elem*
0	0
1	2
2	0
u	x
v	z
w	y
x	u
y	w
z	v

Inverse

Evaluation Methodology
Simulation Infrastructure

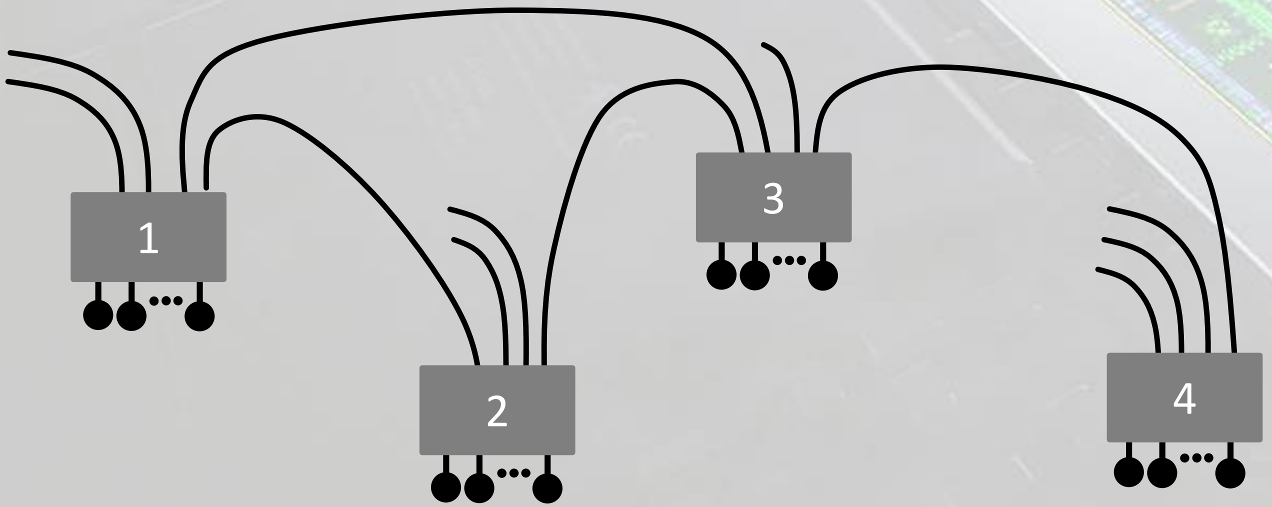


Evaluation Methodology

Simulation Infrastructure

Performance

- **Cycle-accurate simulations (in-house simulator [1], Booksim [2])**



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Evaluation Methodology
Simulation Infrastructure

Performance

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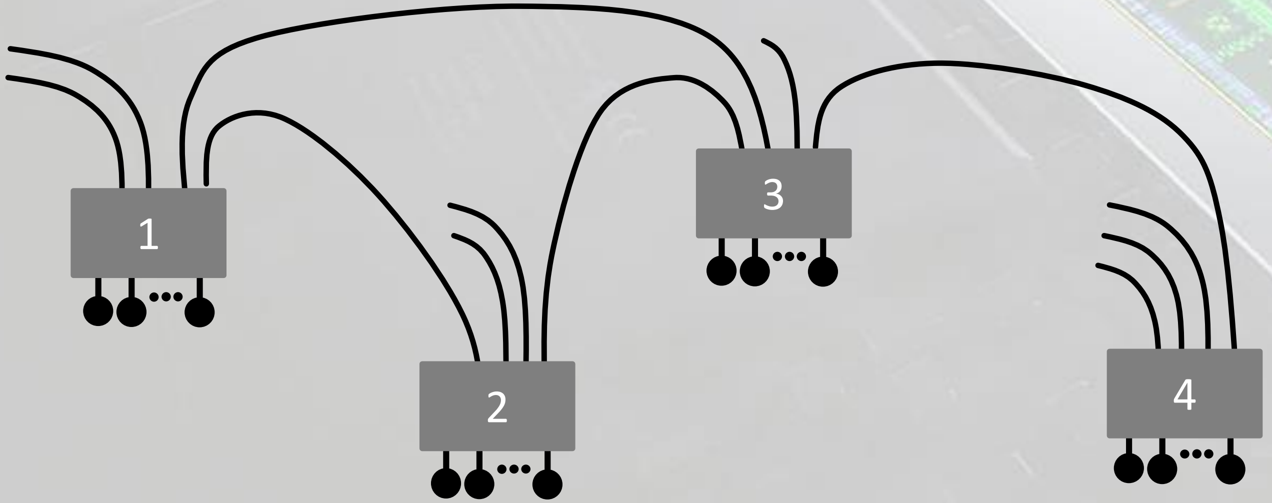

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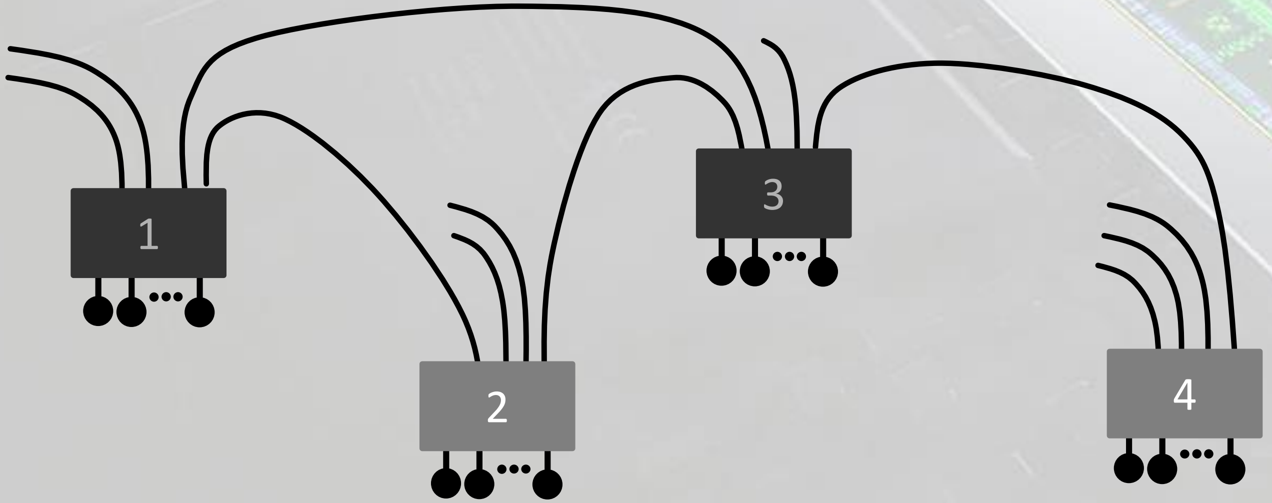

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Evaluation Methodology
Simulation Infrastructure

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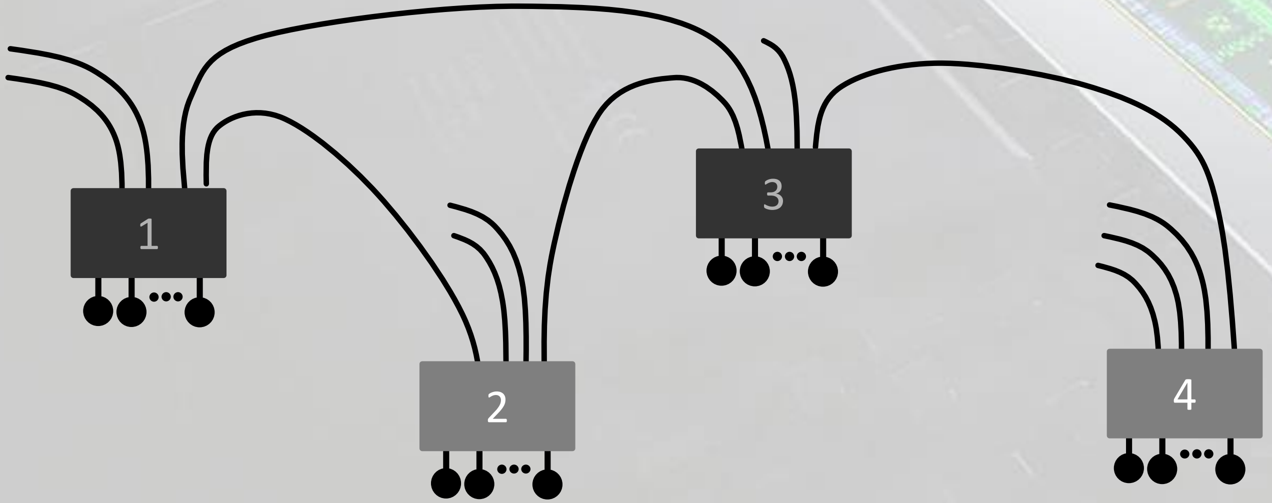
- **Cycle-accurate simulations (in-house simulator [1], Booksim [2])**
- Routing protocols:
  - Minimum static routing



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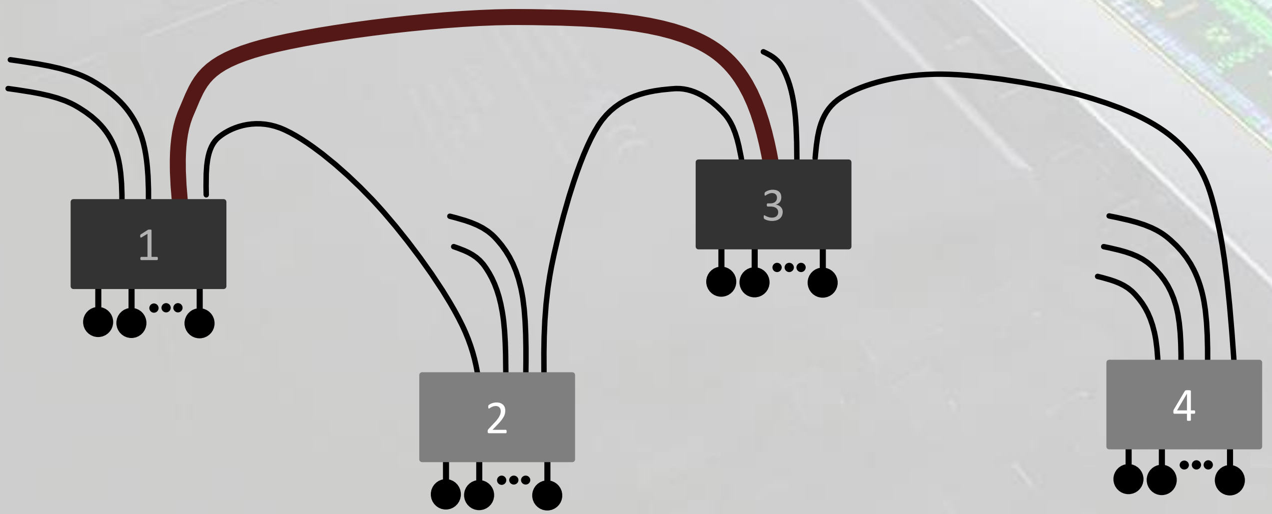

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Evaluation Methodology

Simulation Infrastructure

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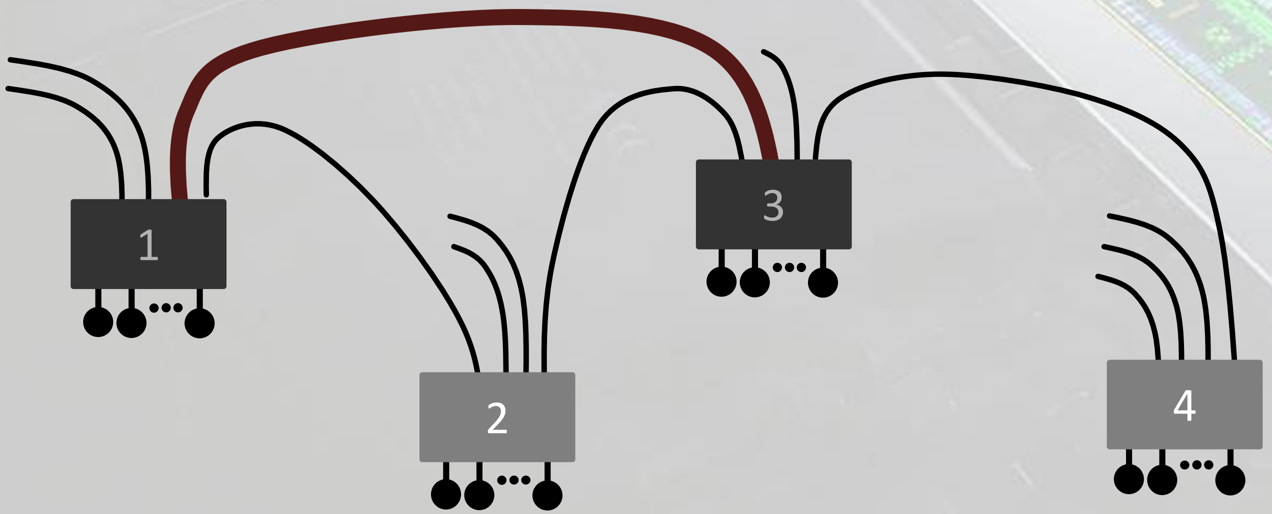

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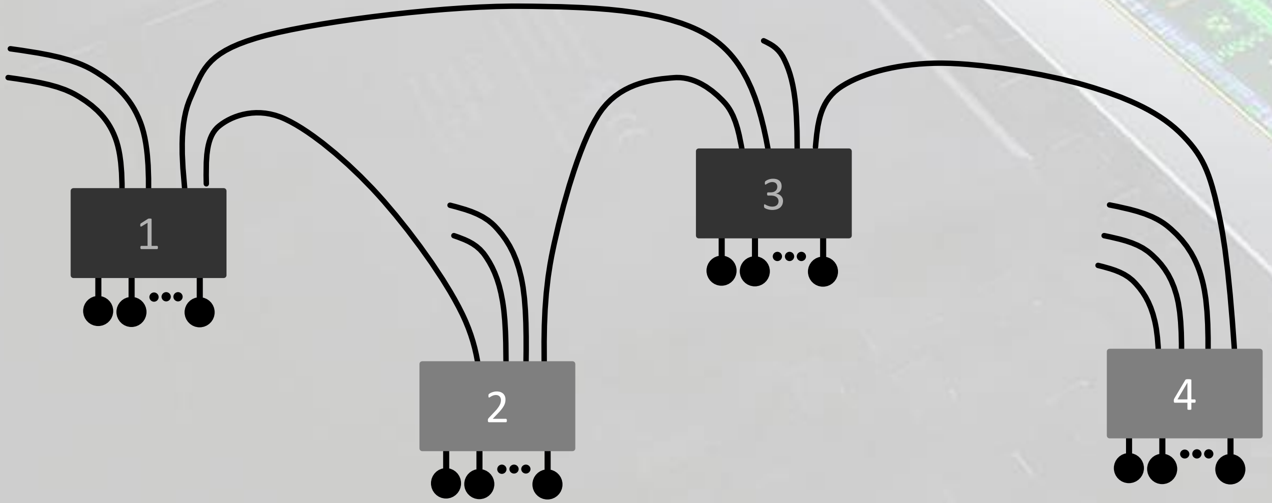

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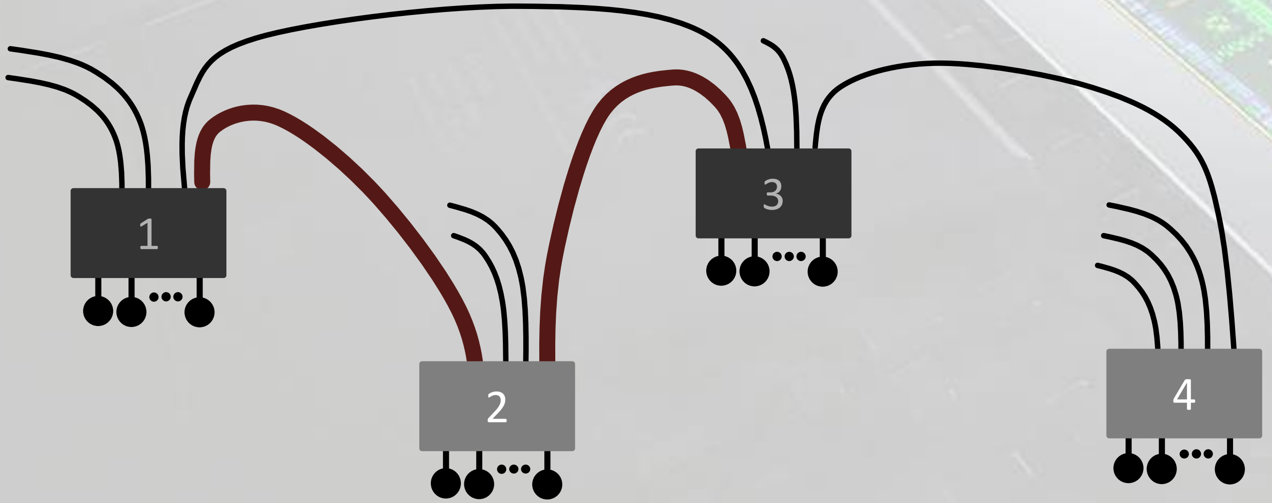

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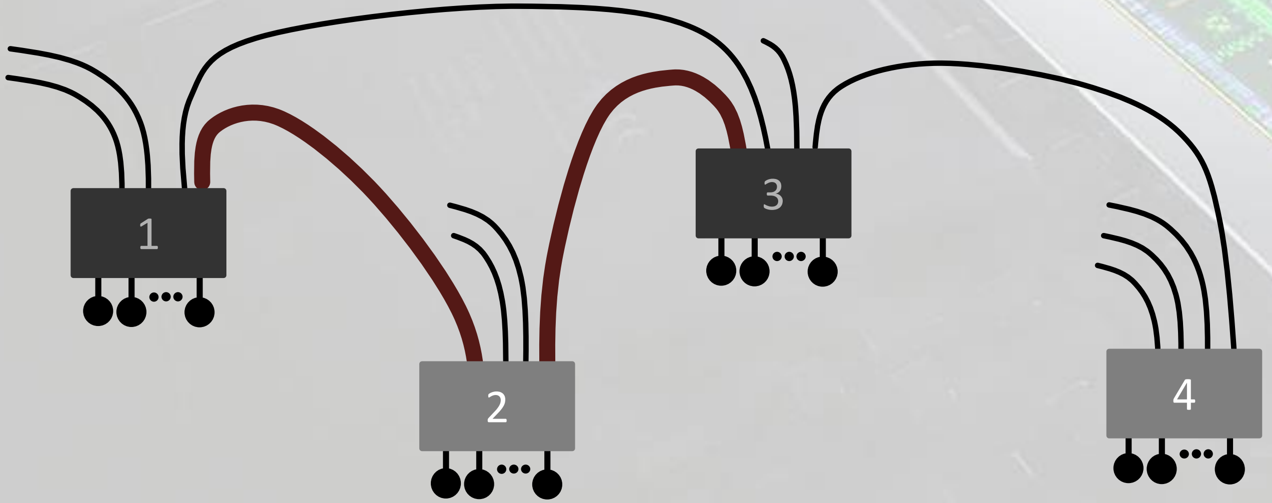

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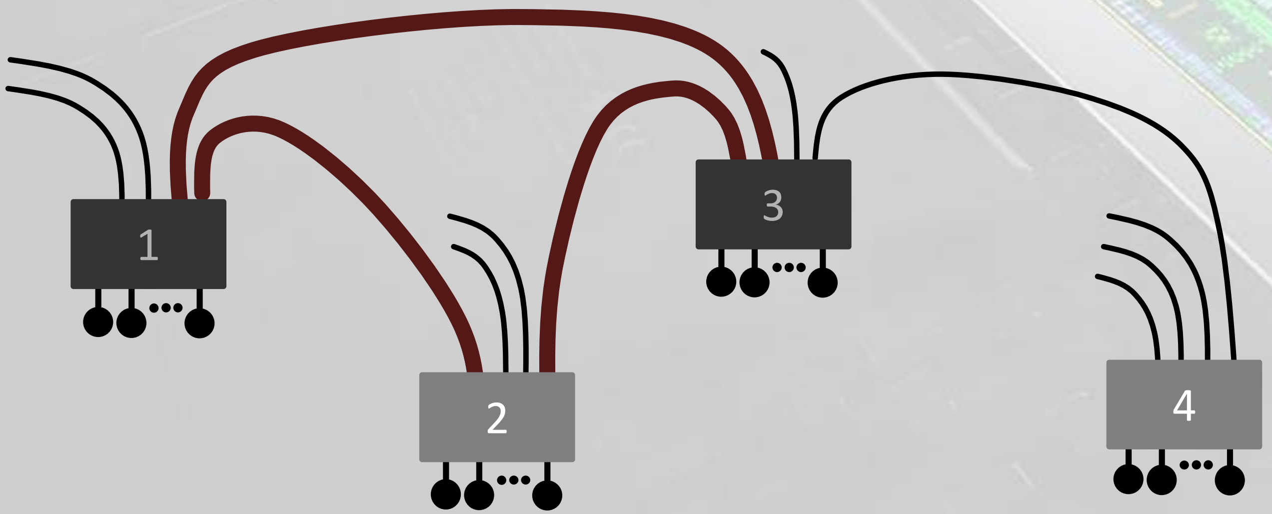

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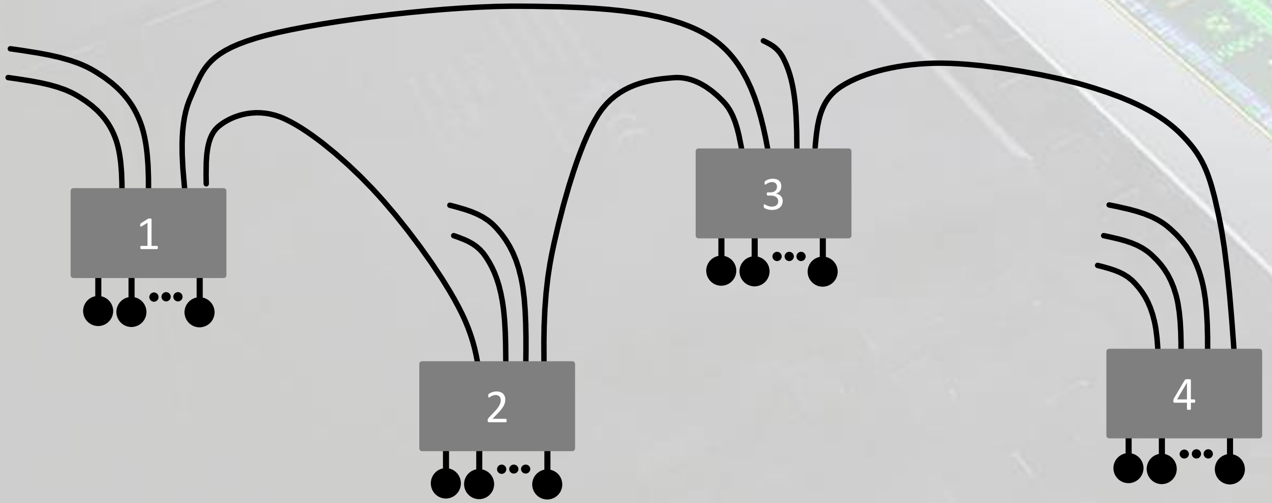

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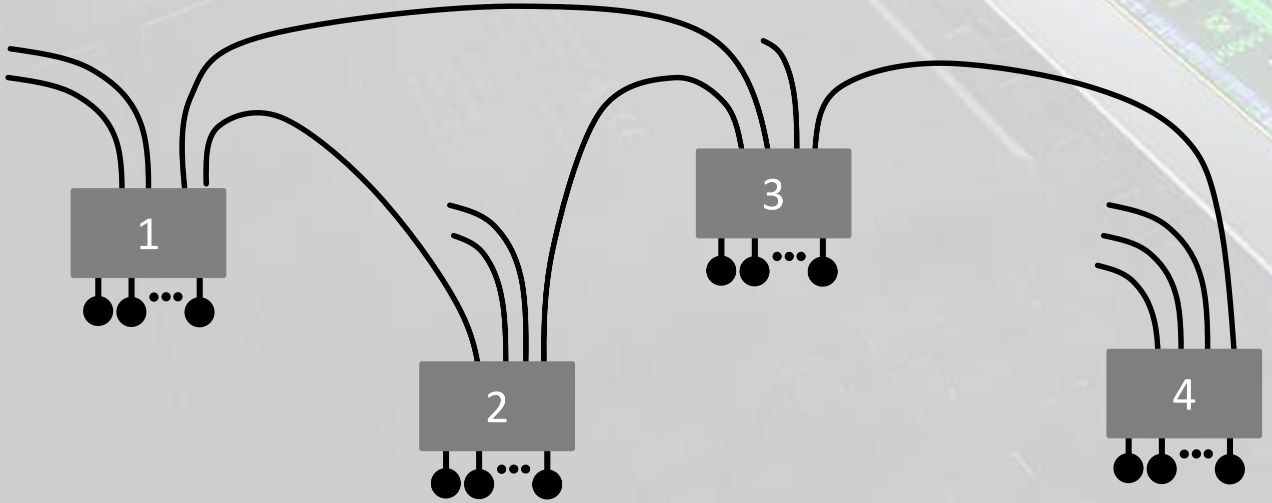
    UGAL-L: each router has access to its local output queues



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Evaluation Methodology
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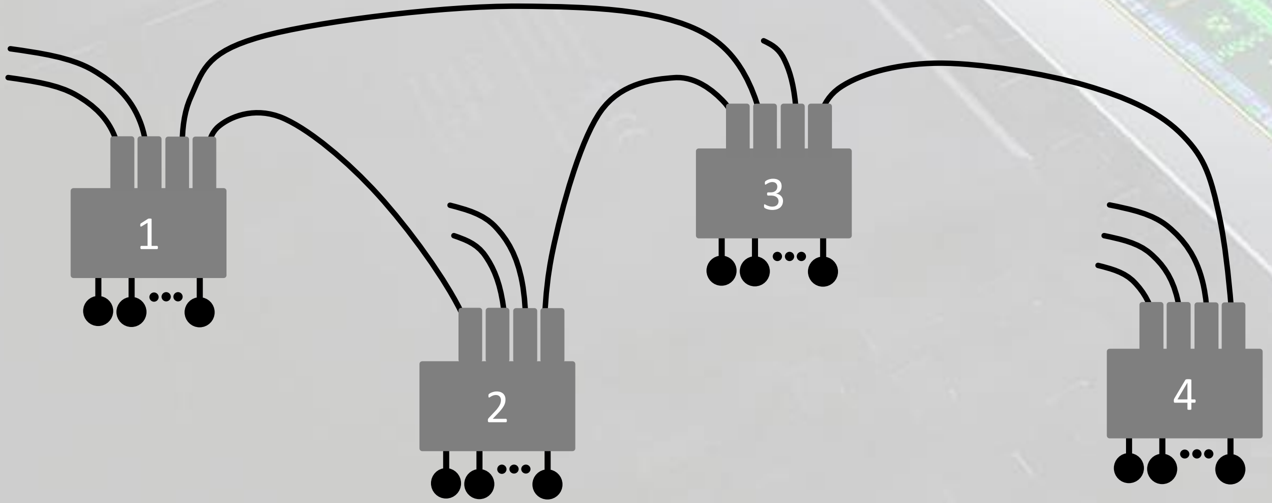

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Evaluation Methodology

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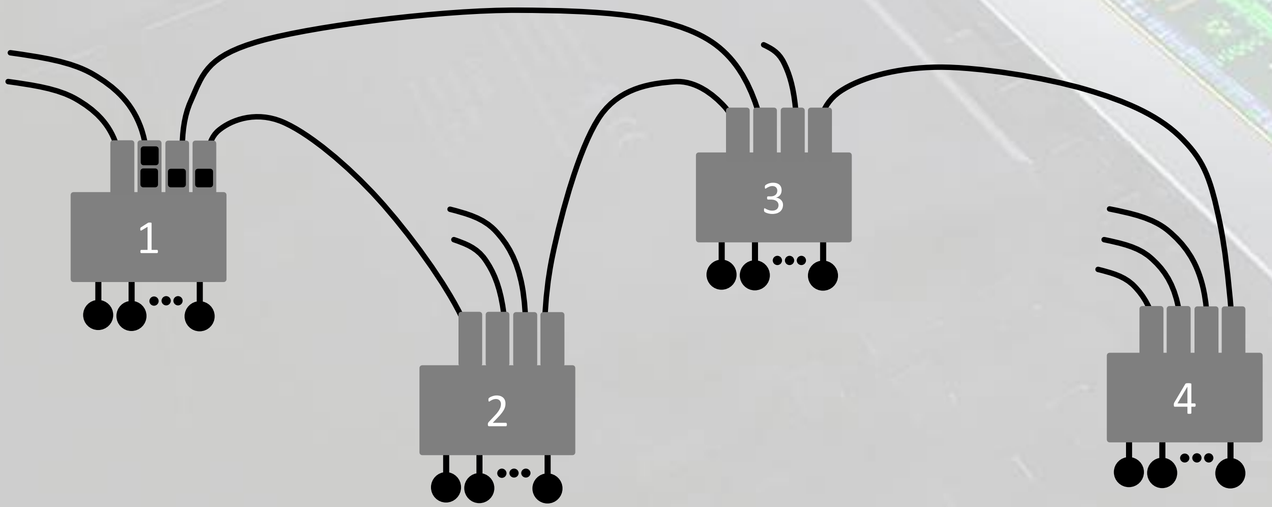

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EVALUATION METHODOLOGY
SIMULATION INFRASTRUCTURE

PERFORMANCE

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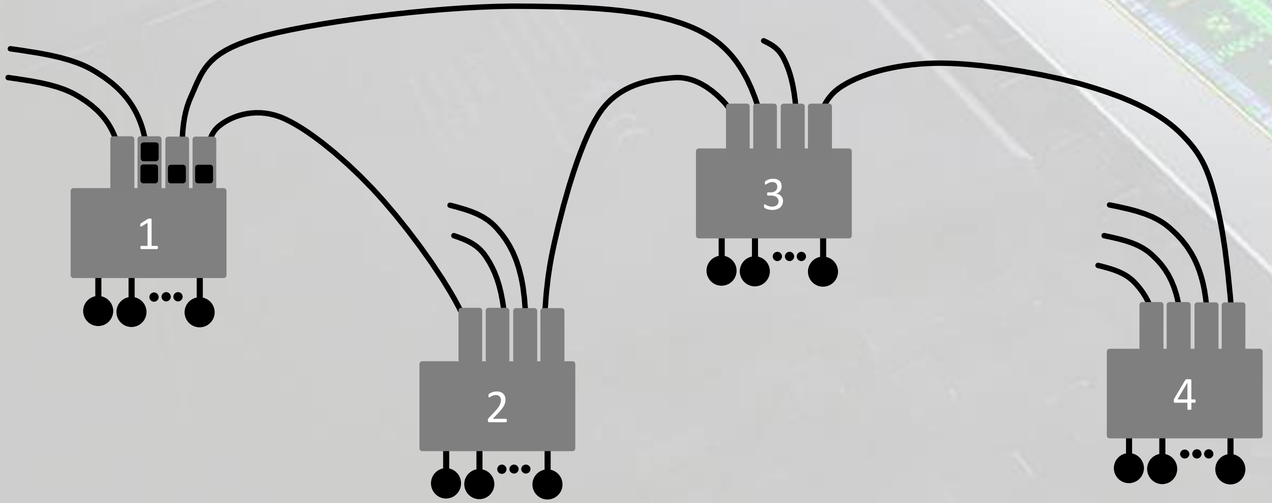
- Routing protocols:
  - Minimum static routing
  - Valiant routing [3]
  - Universal Globally-Adaptive Load-Balancing routing [4]
    UGAL-L: each router has access to its local output queues
    UGAL-G: each router has access to the sizes of all the queues



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Evaluation Methodology

Simulation Infrastructure

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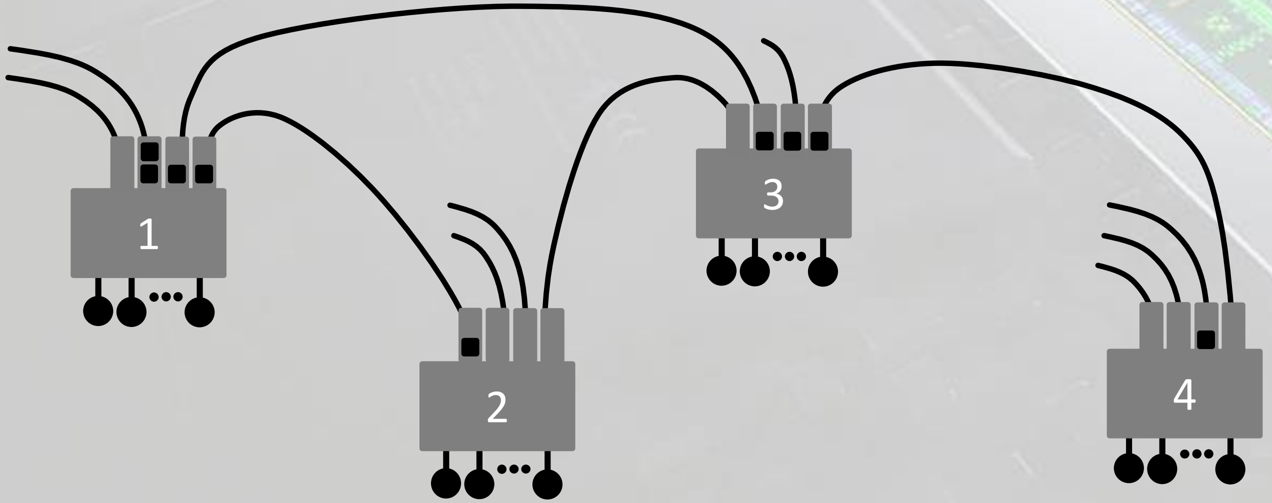

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Evaluation Methodology
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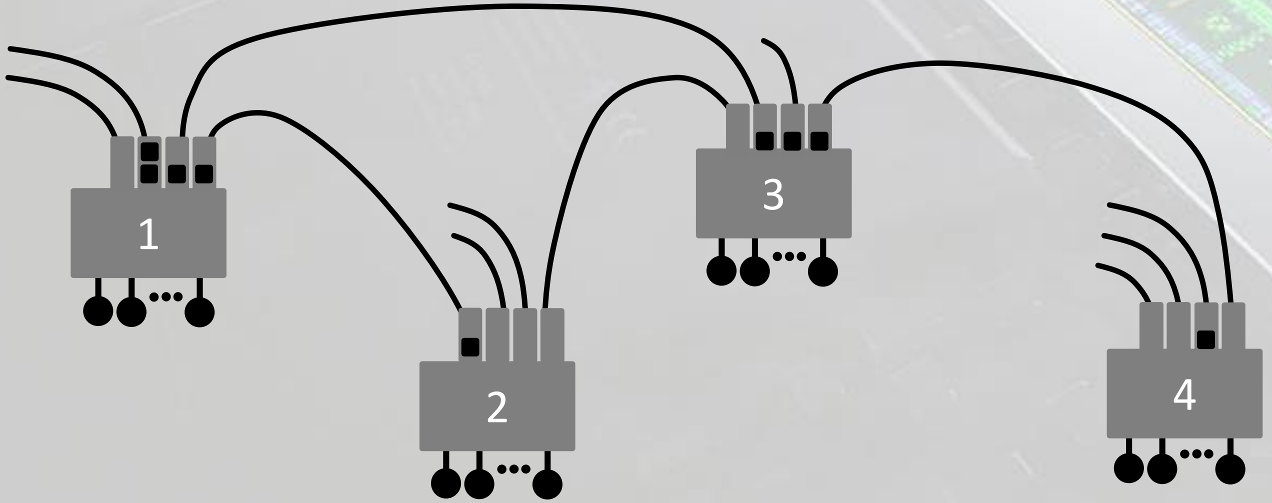

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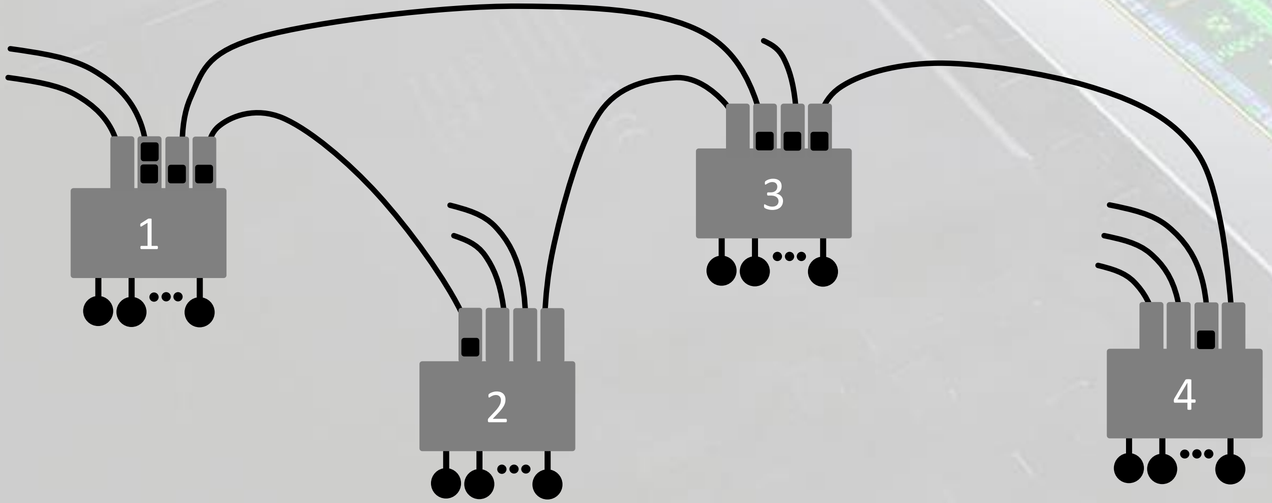

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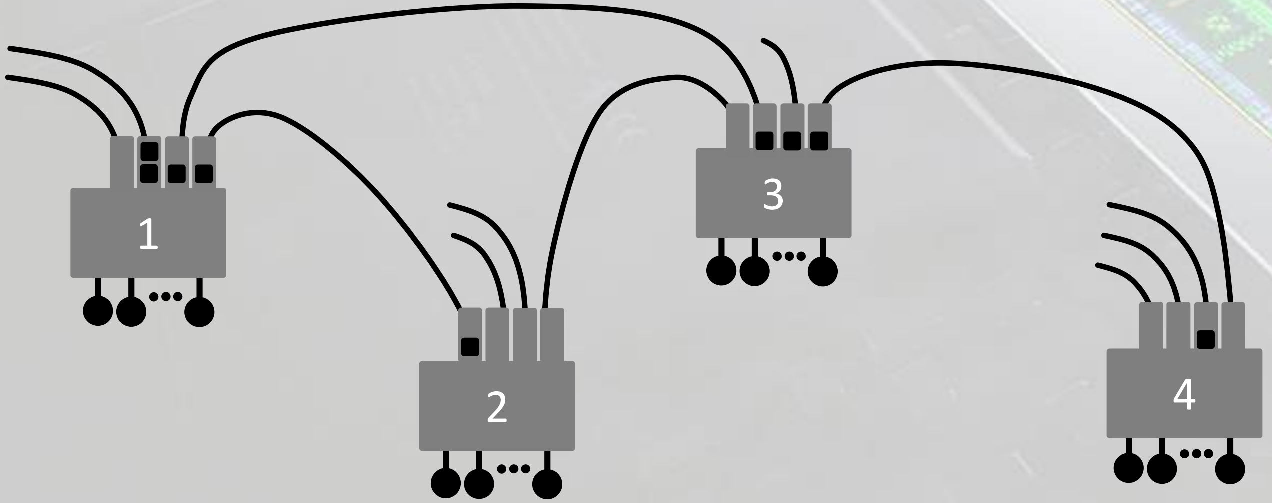

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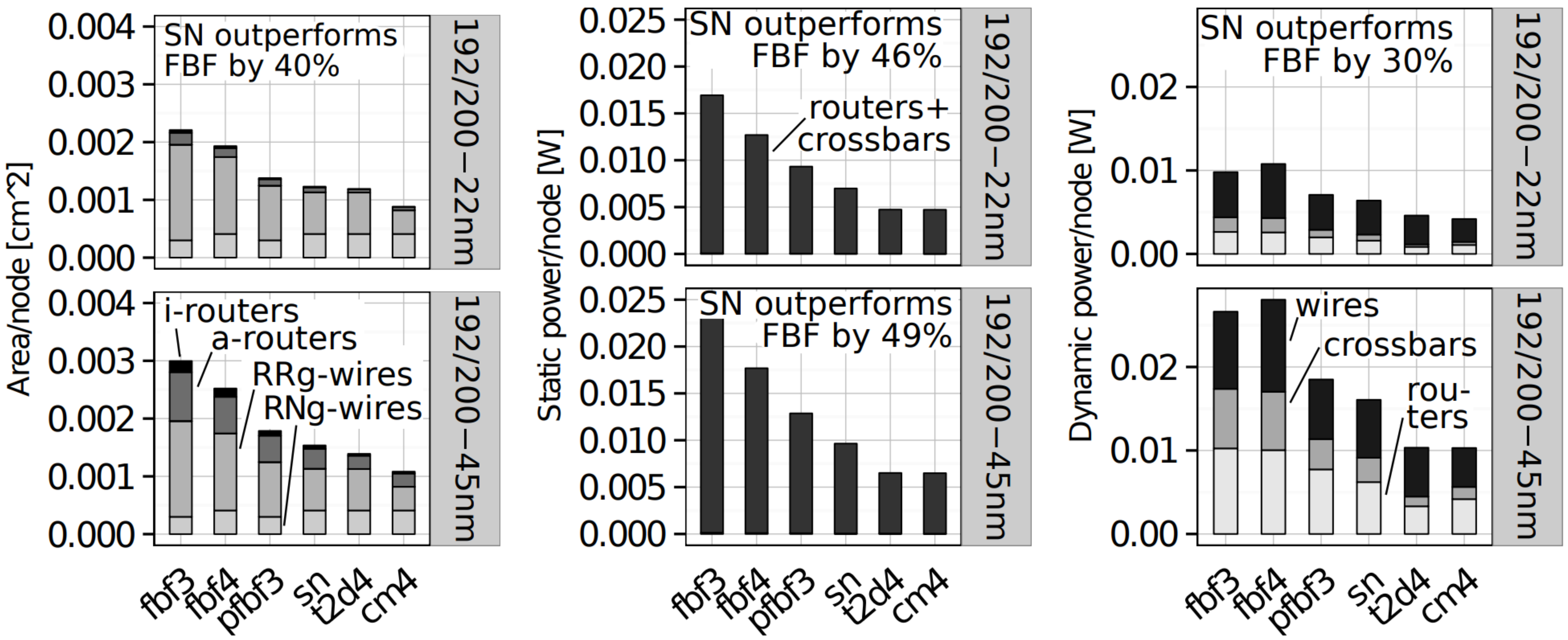
Results: Area and Power Consumption

Smart links: ON
Central Buffers: ON
Node count: 192/200



(a) Area. **(b)** Static power. **(c)** Dynamic power.

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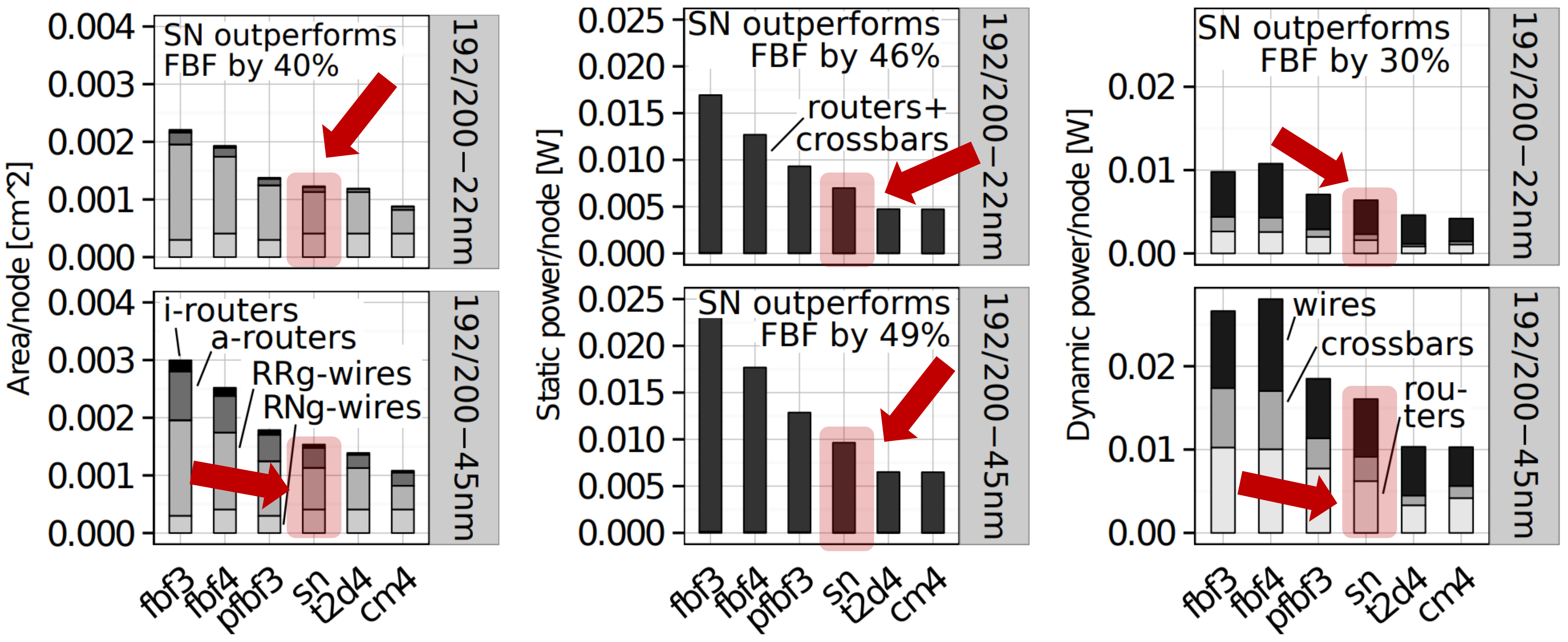

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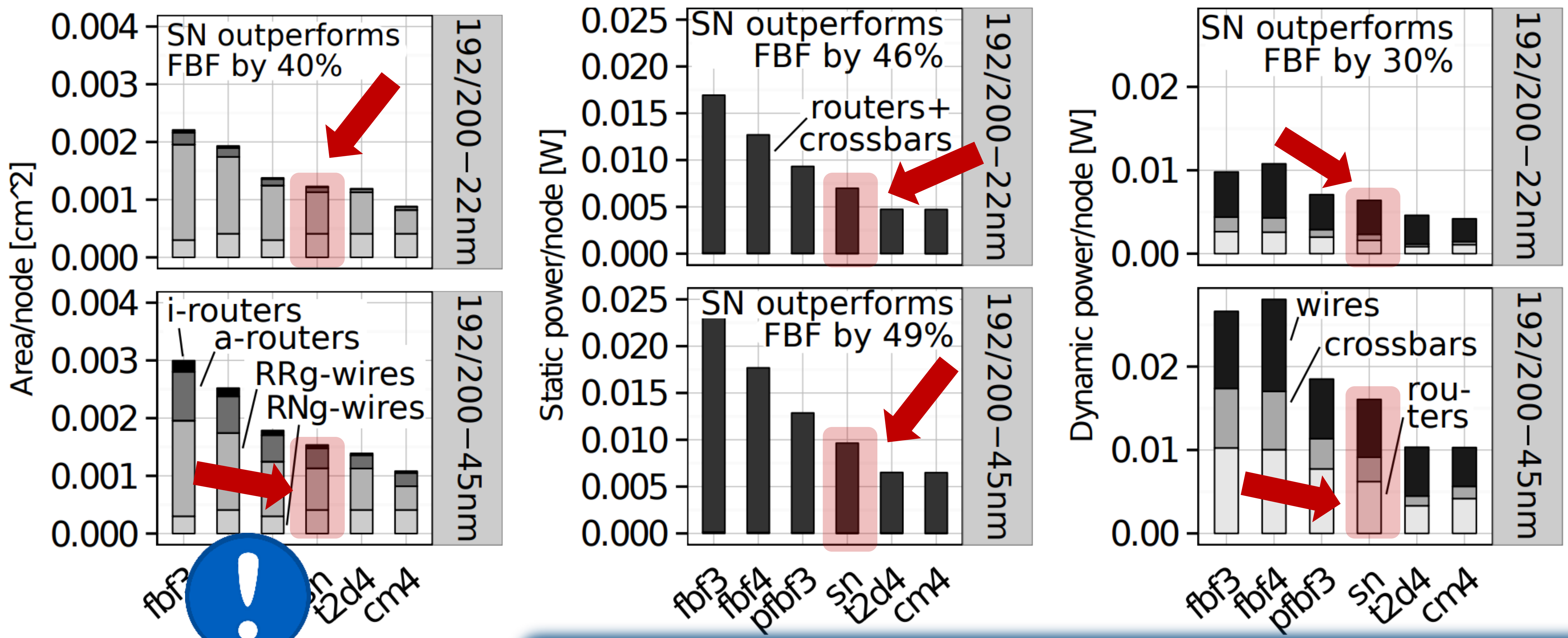
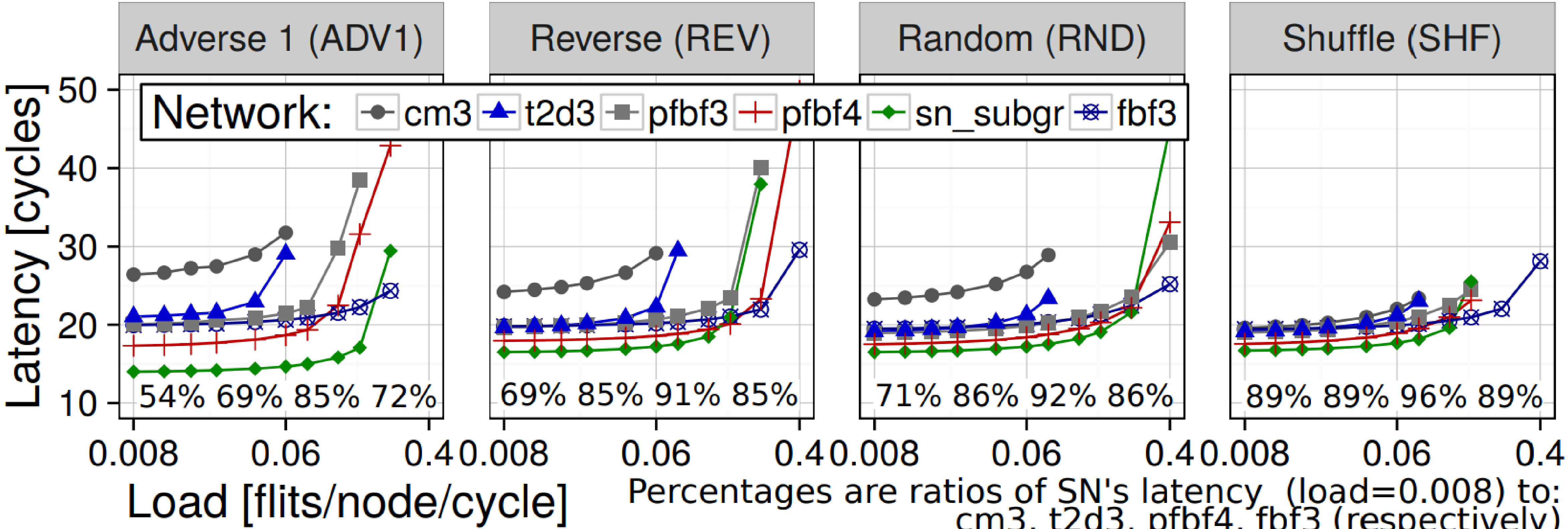


(a) Area.

Slim NoC is more efficient than high-radix

Results: Performance

Smart links: ON
Central Buffers: ON
Node count: 192/200



Percentages are ratios of SN's latency (load=0.008) to: cm3, t2d3, pfbf4, fbf3 (respectively)

RESULTS: PERFORMANCE

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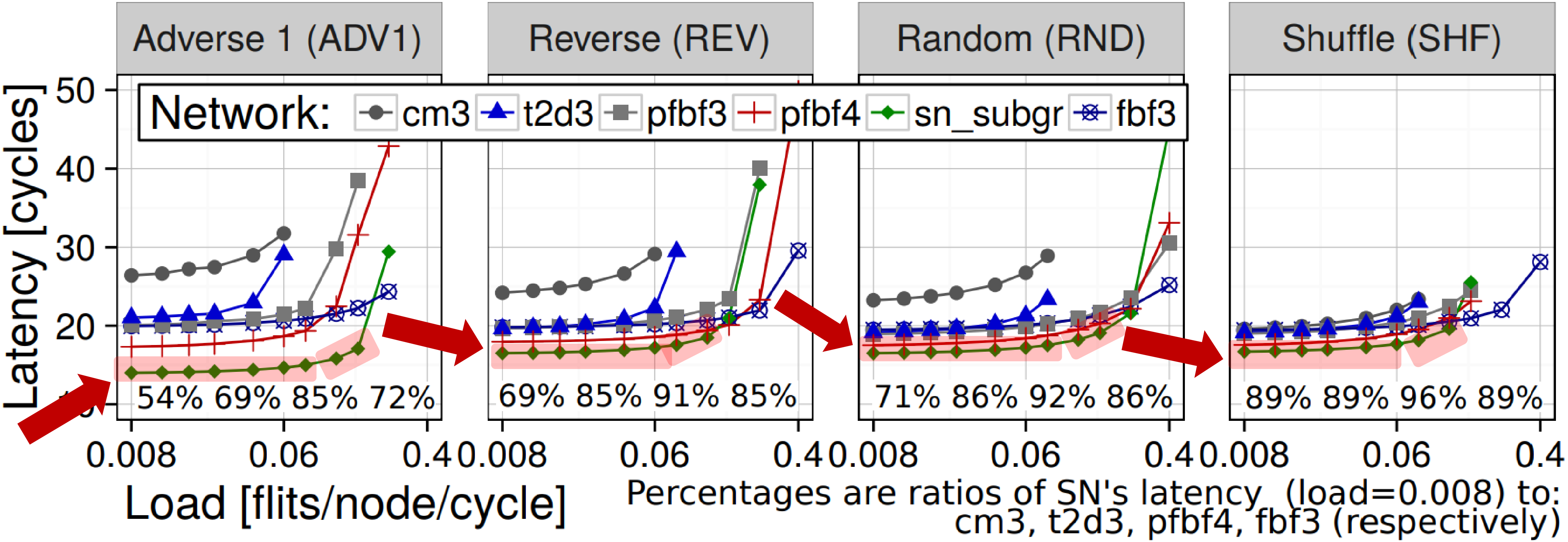

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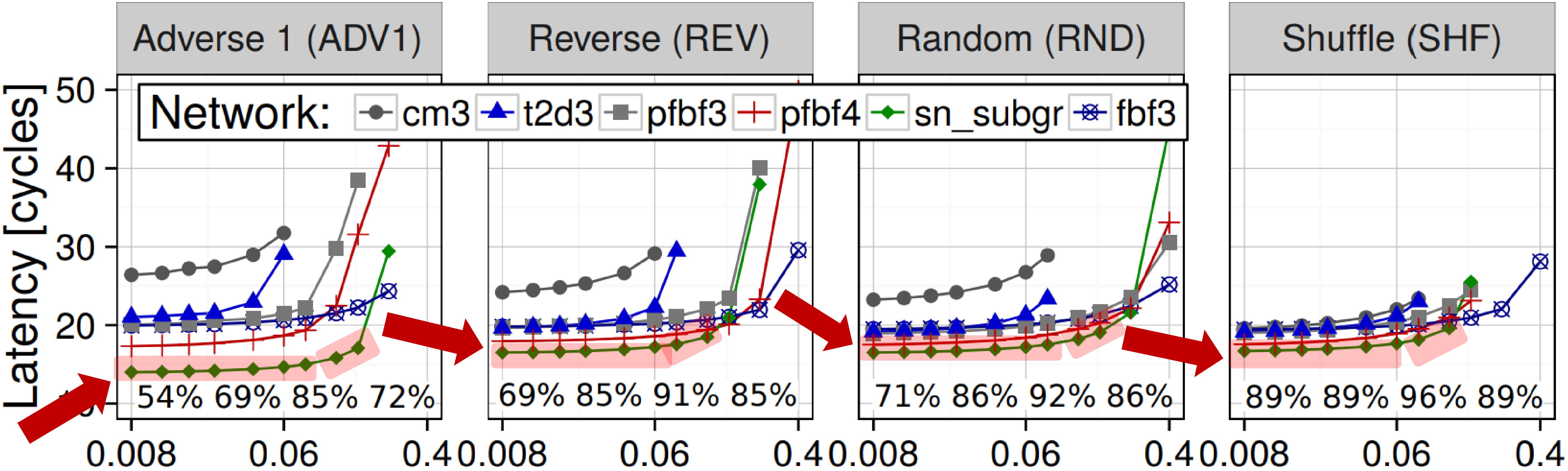

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Slim NoC ensures the lowest latency

Evaluation

Selected other insights

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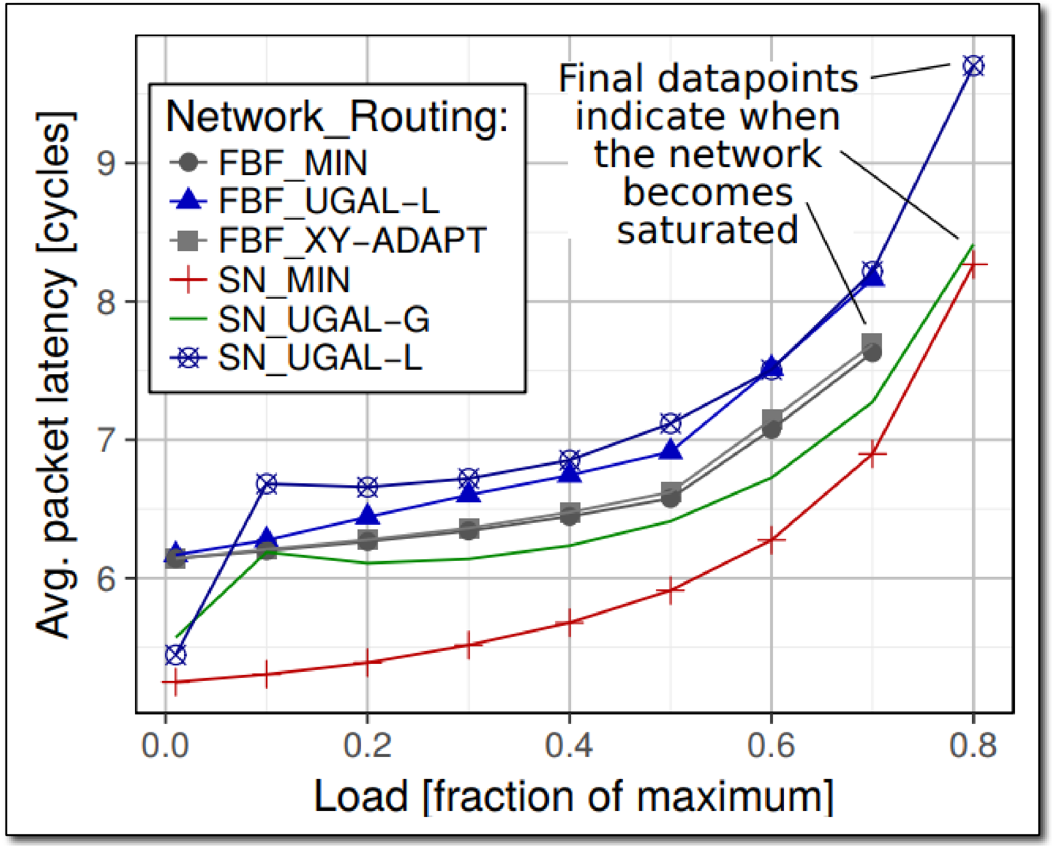
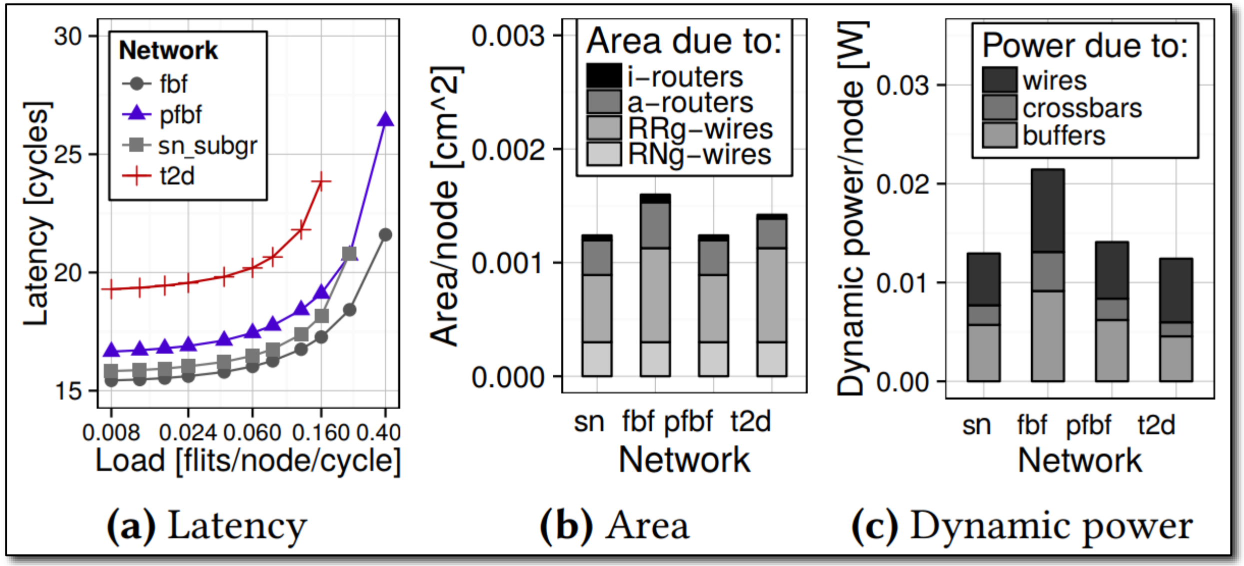


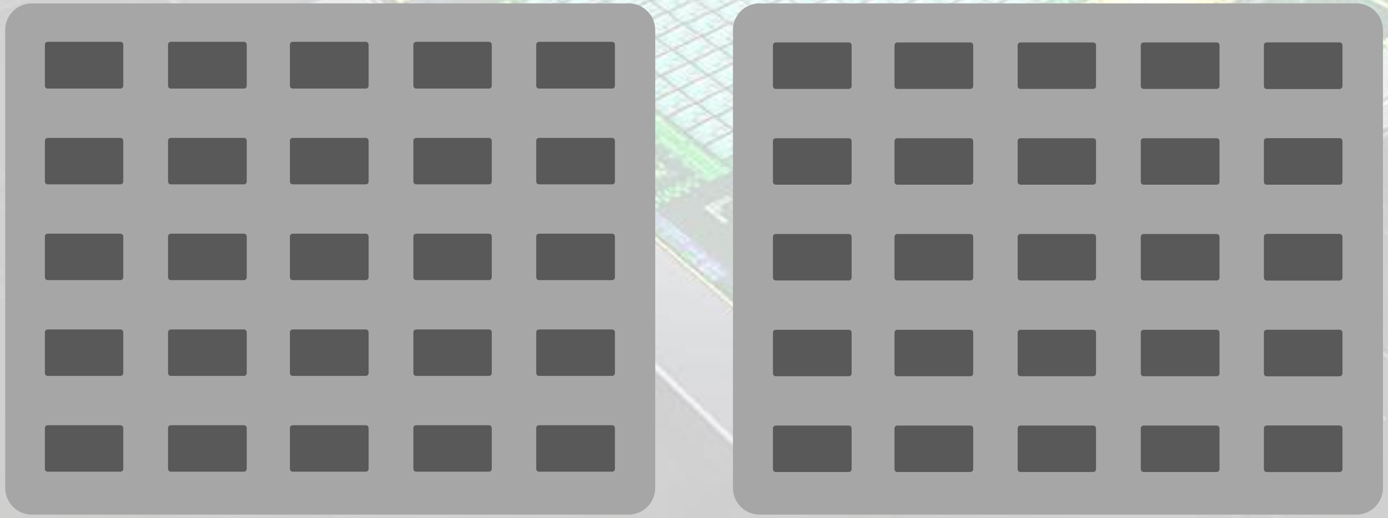
Node count: 192/200

Node count: 54



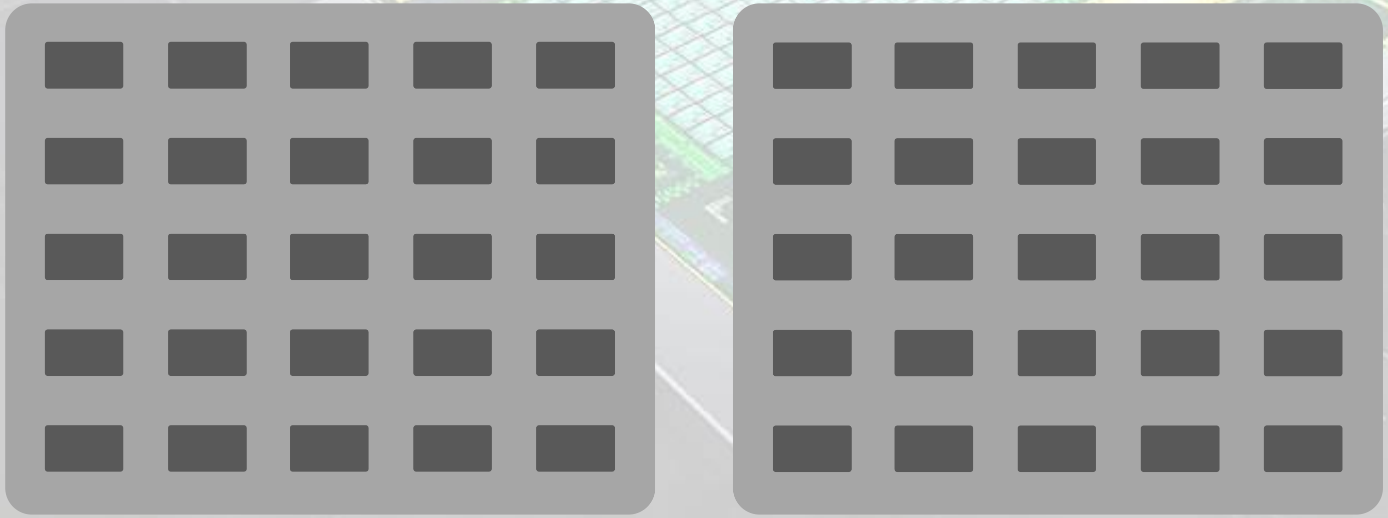
(a) Latency (b) Area (c) Dynamic power

Performance & routing
Minimum routing



Performance & routing
Minimum routing

❶ *Intra-group connections*



Performance & routing
Minimum routing

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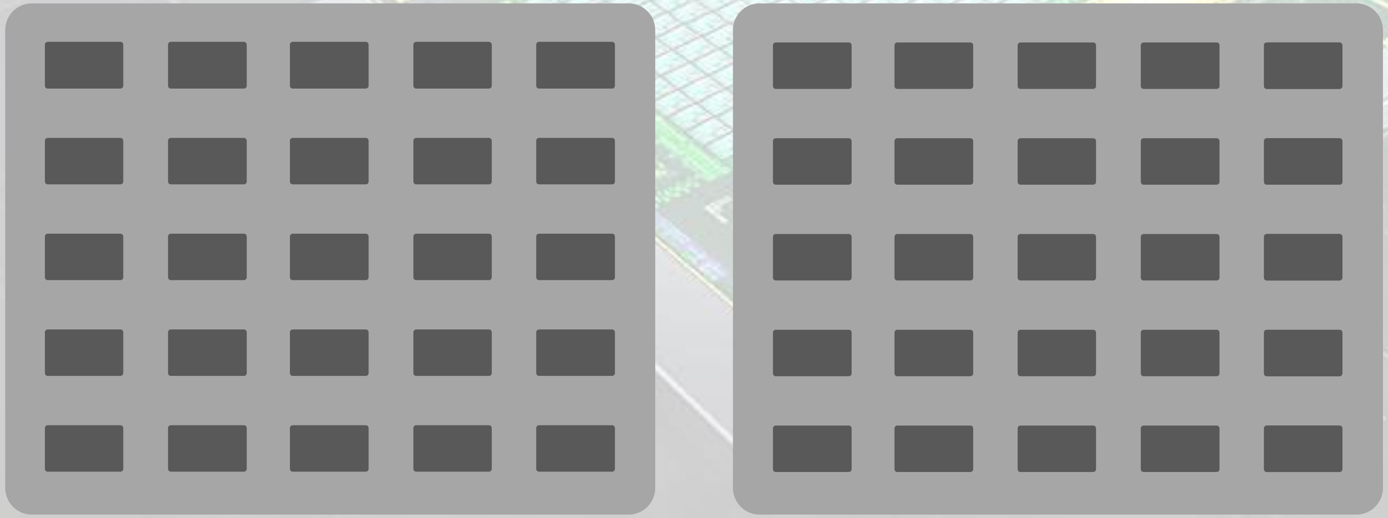

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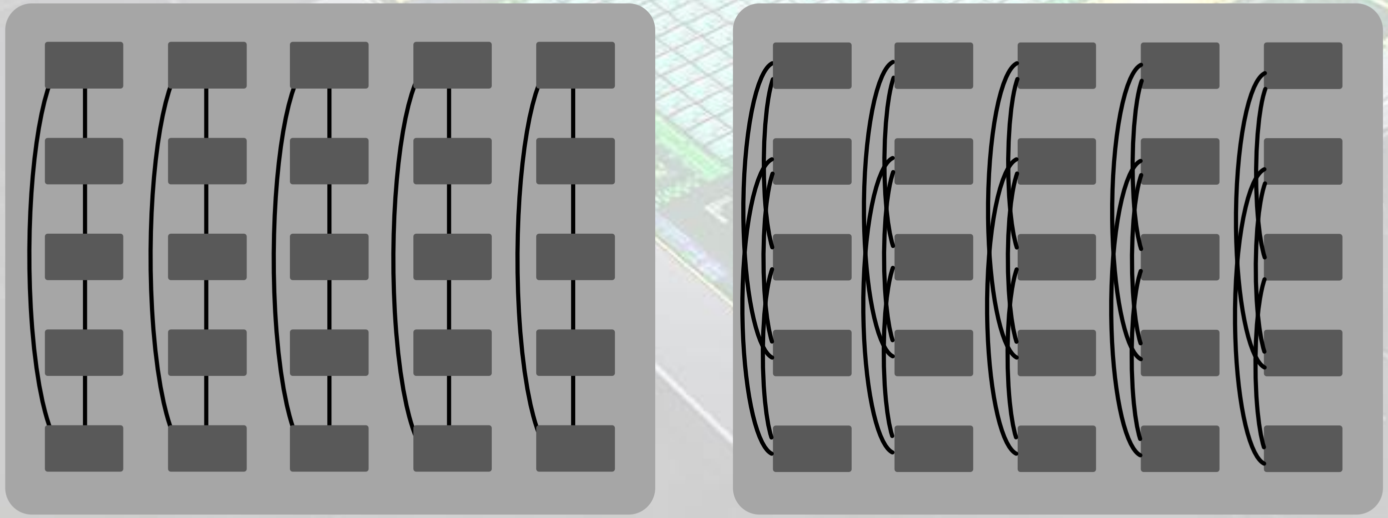

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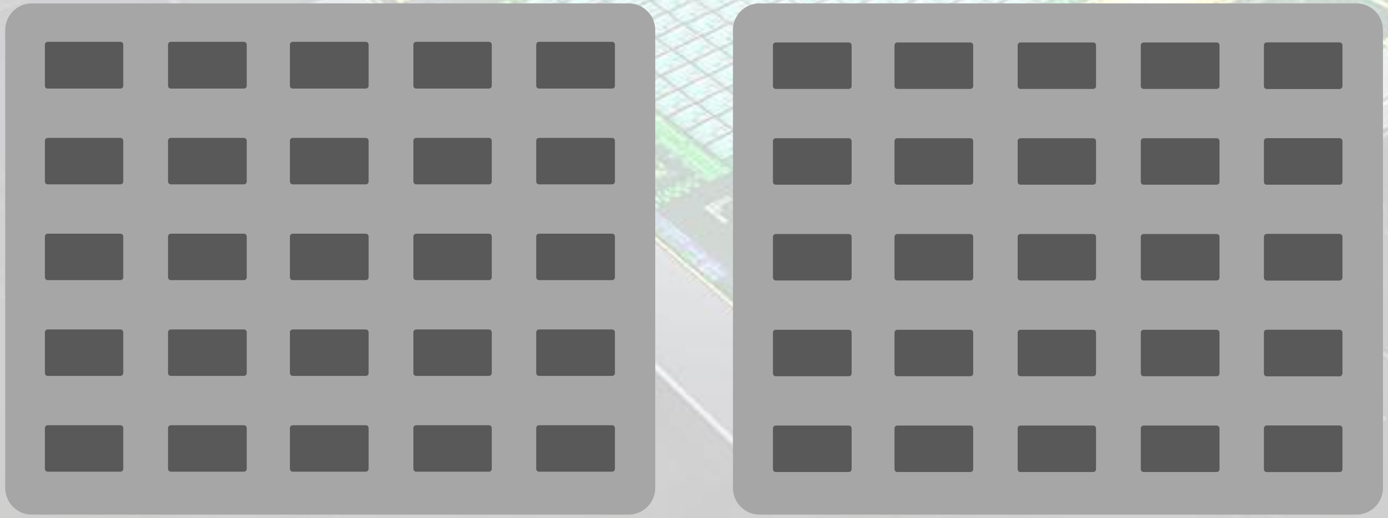

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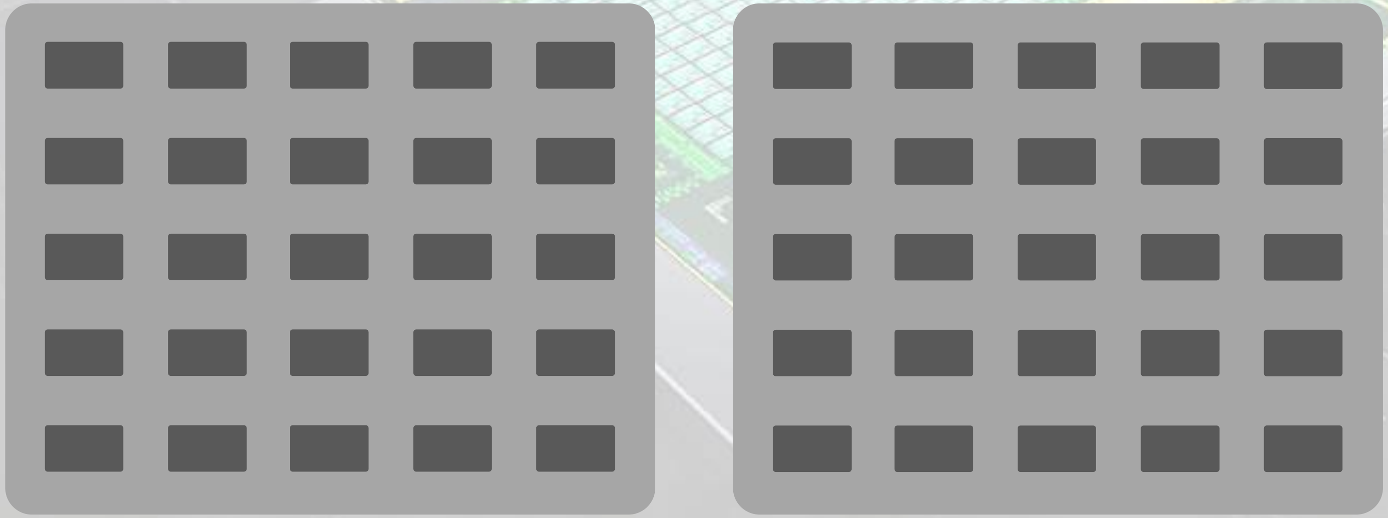

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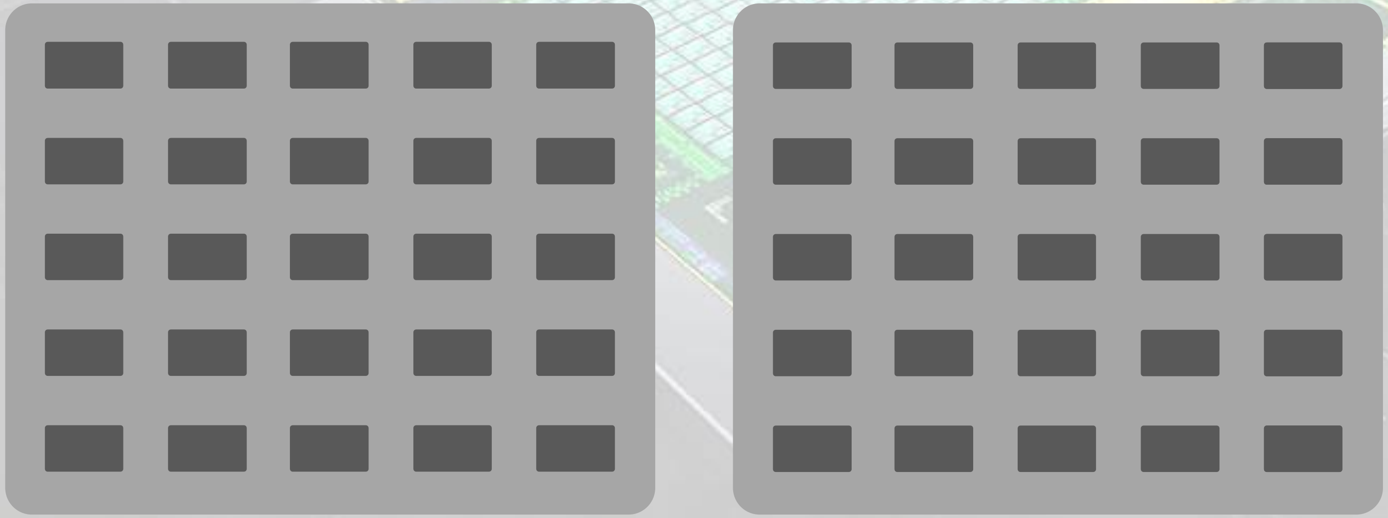

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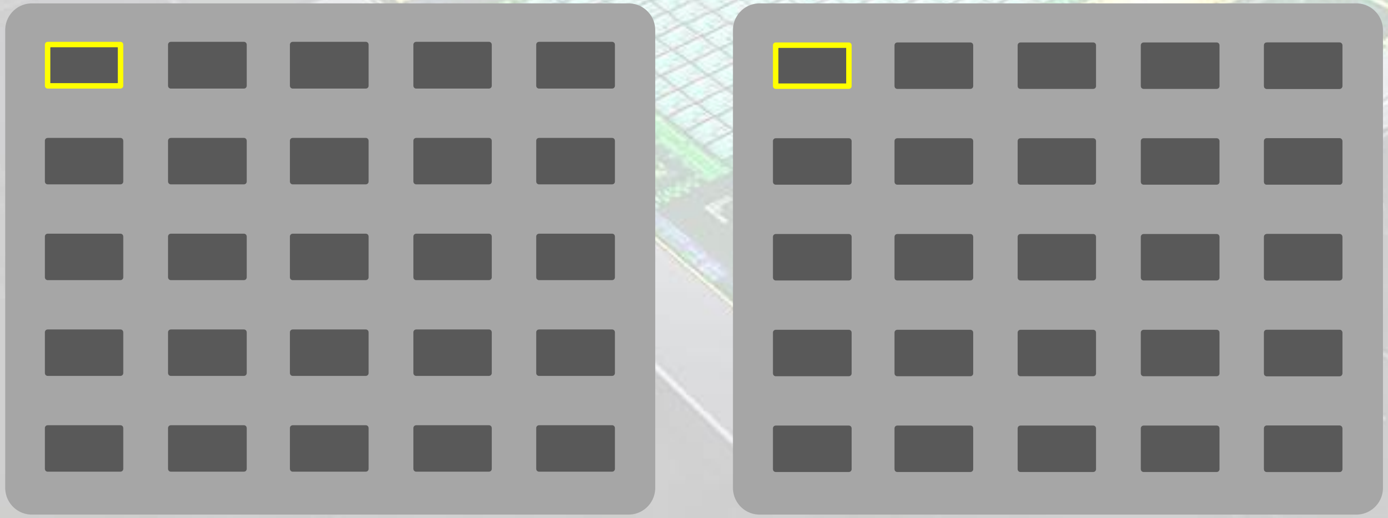

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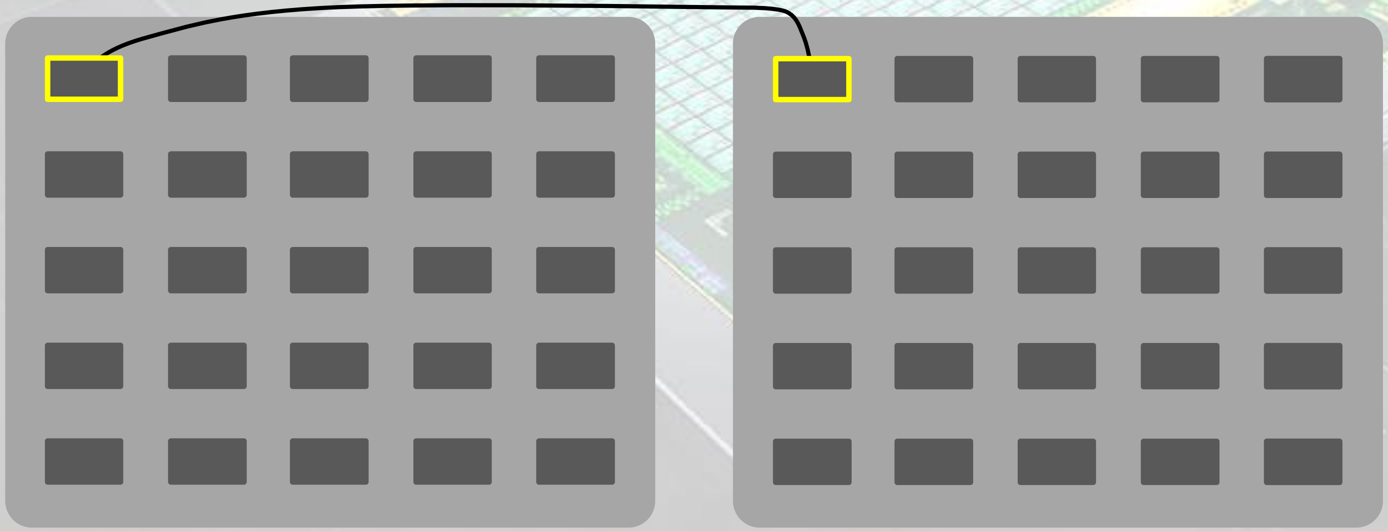

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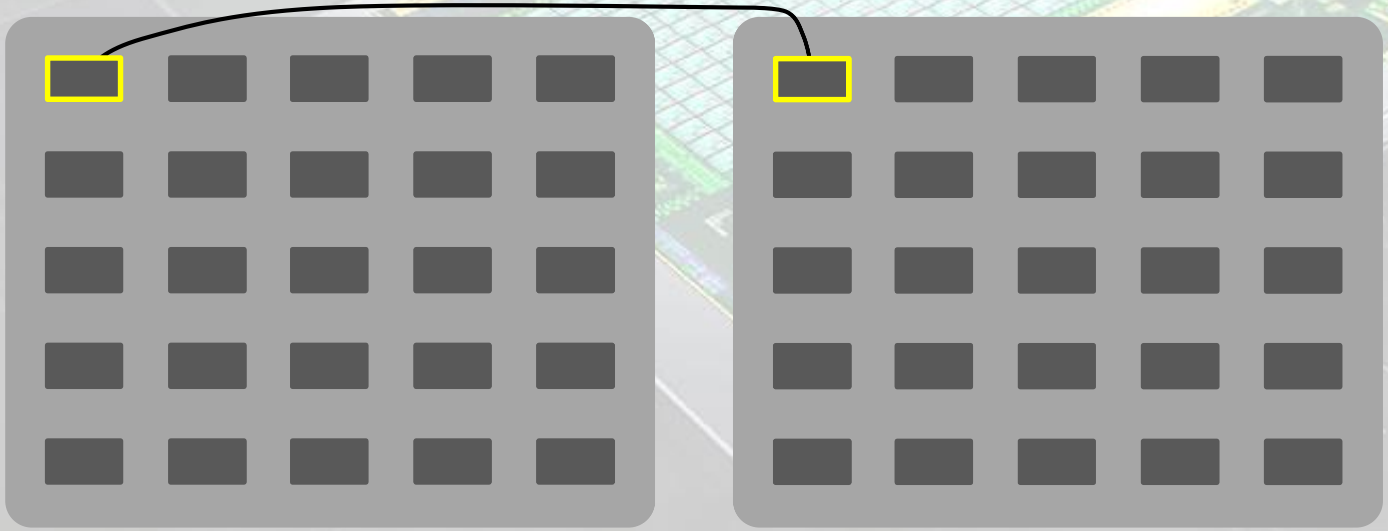

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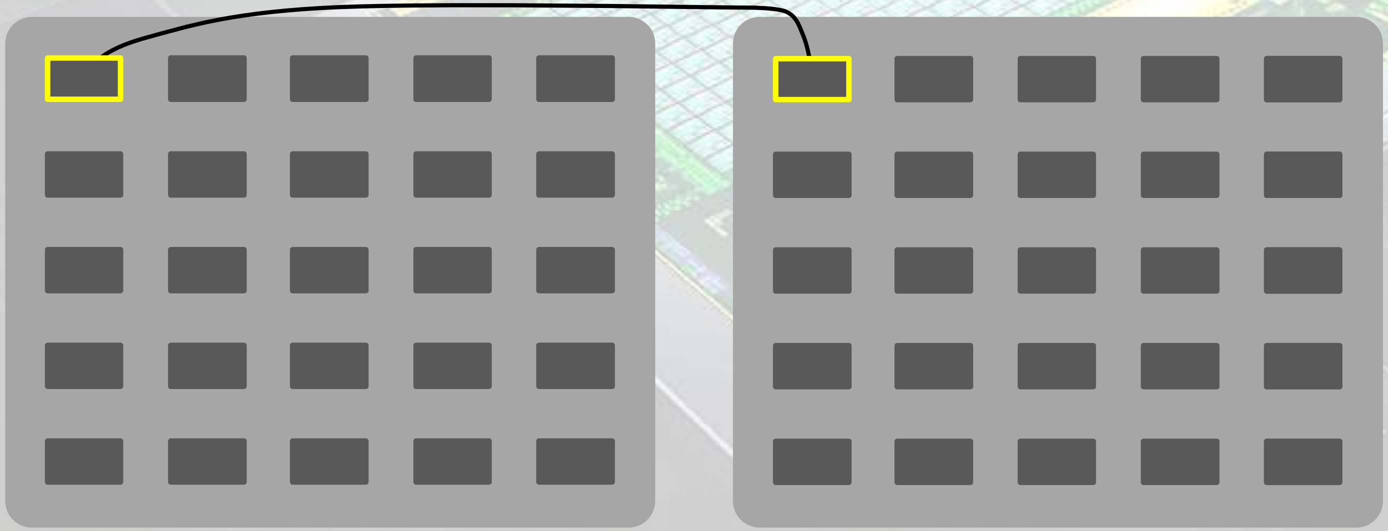

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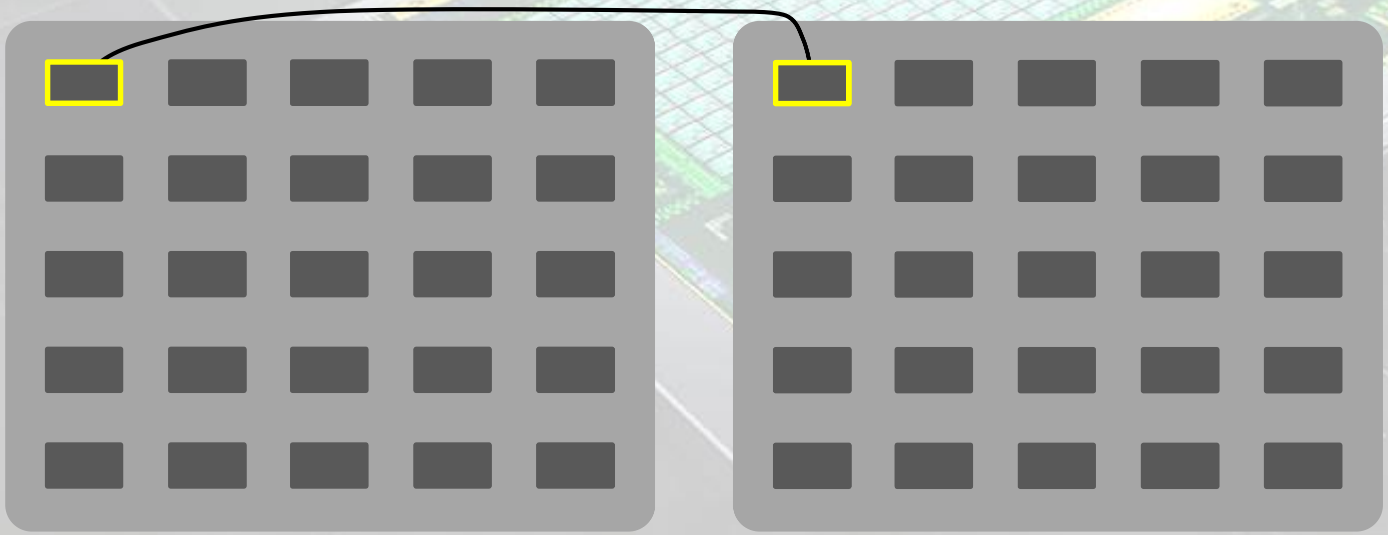
∃ Path of length 2 between two routers



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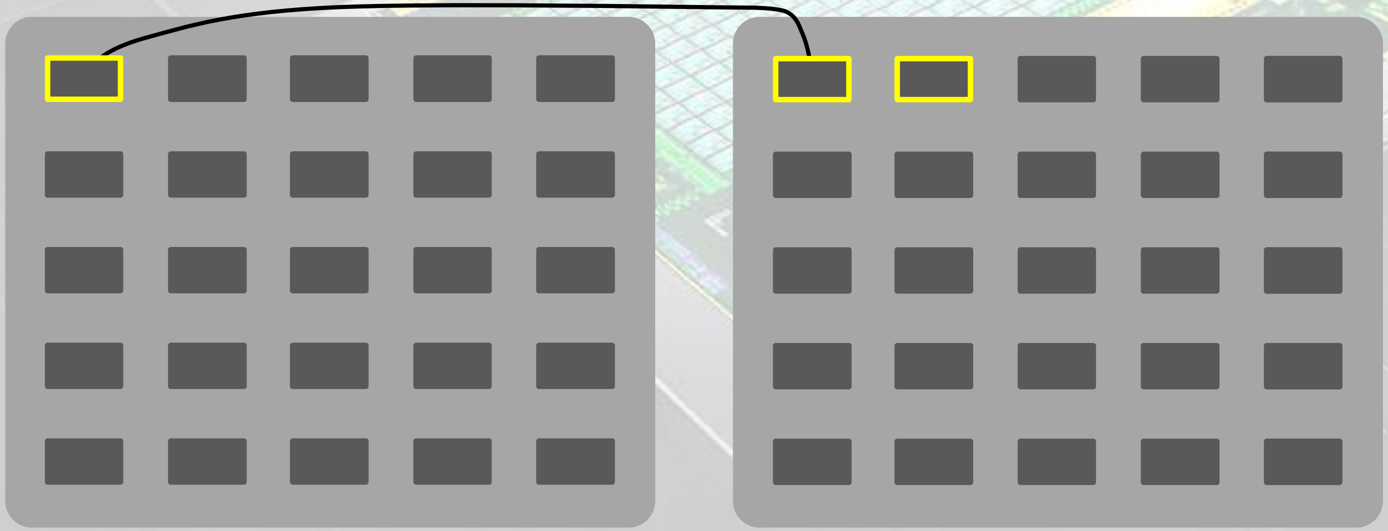

PERFORMANCE & ROUTING
MINIMUM ROUTING

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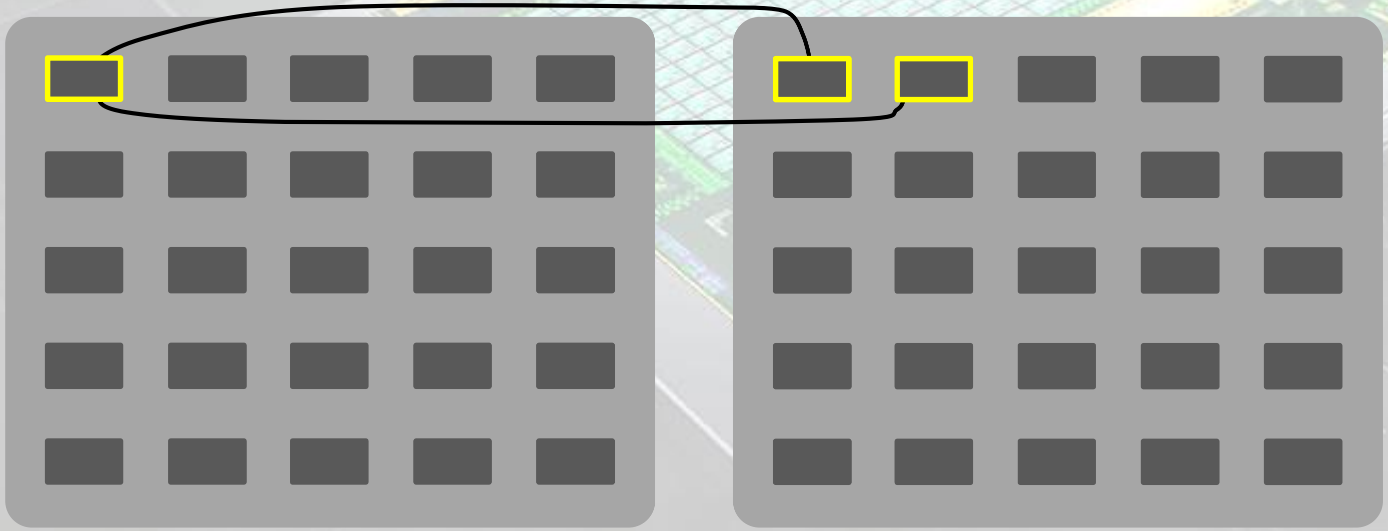

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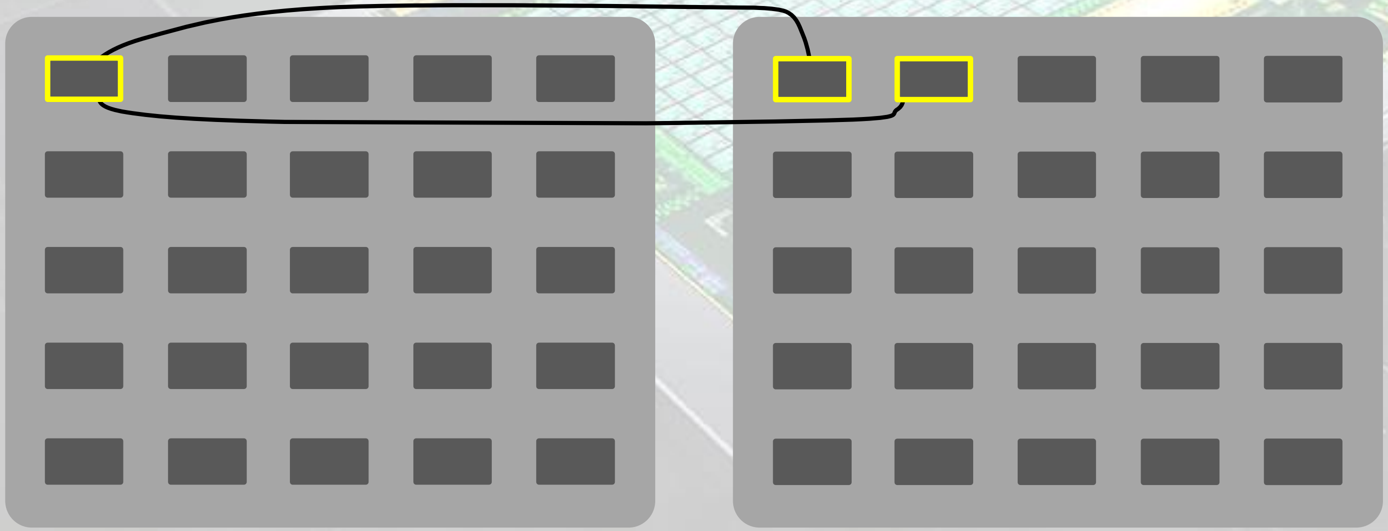

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$$q = 4w + \delta;$$

$$w \in \mathbb{N} \quad \delta \in \{-1, 0, 1\},$$

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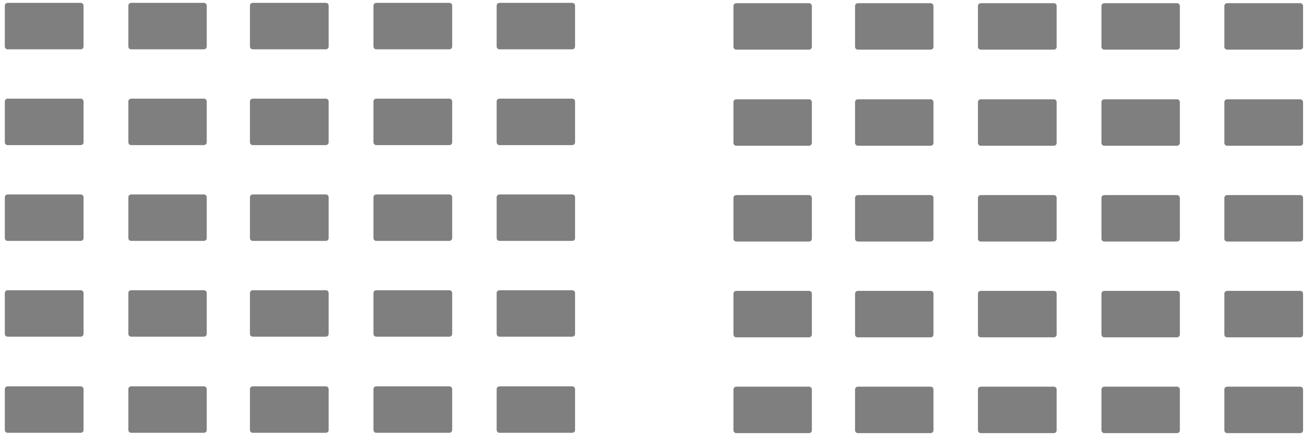

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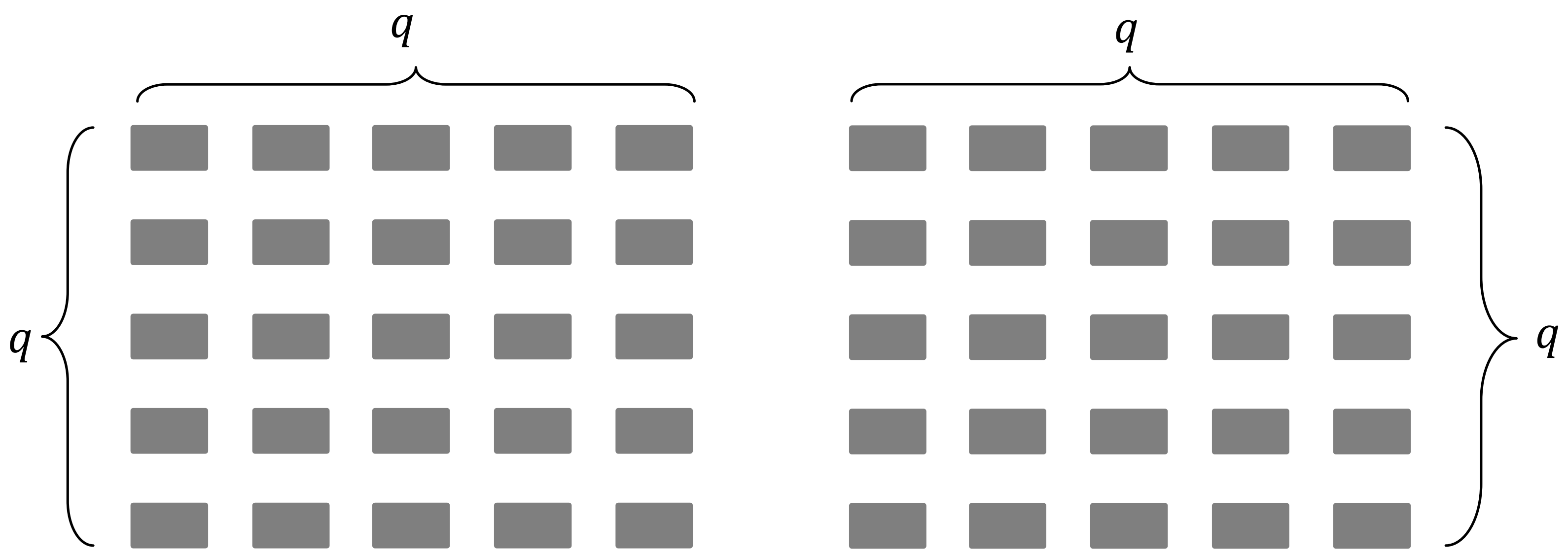

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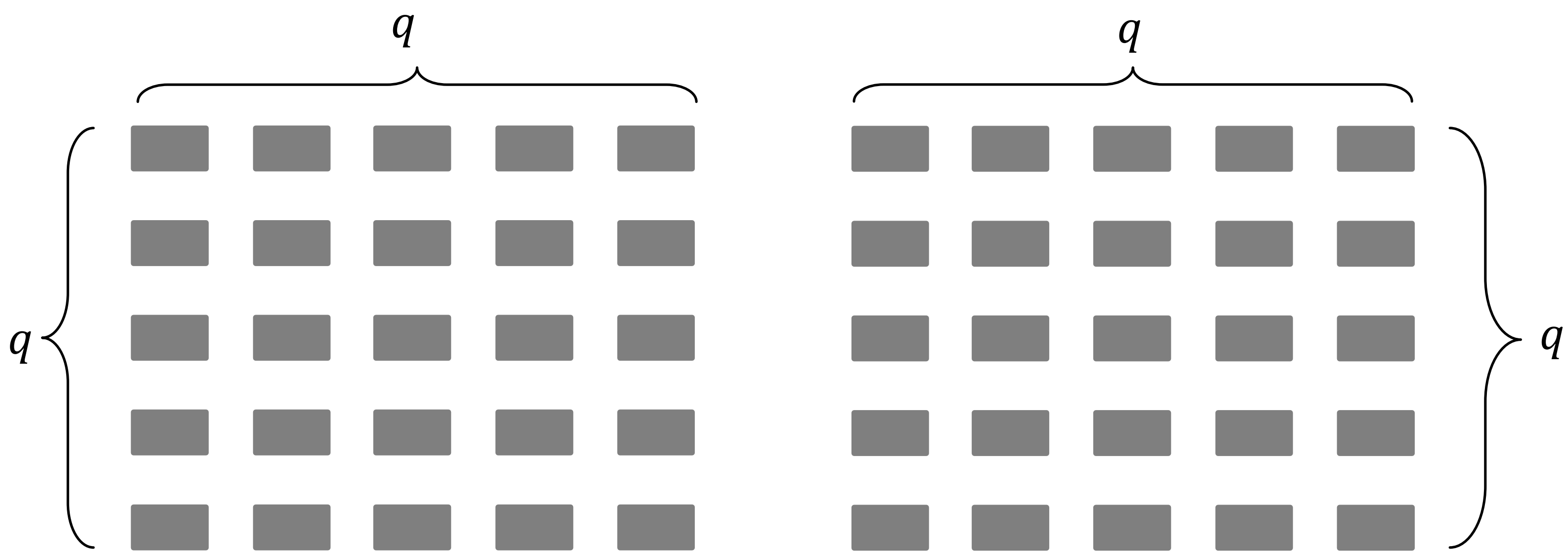

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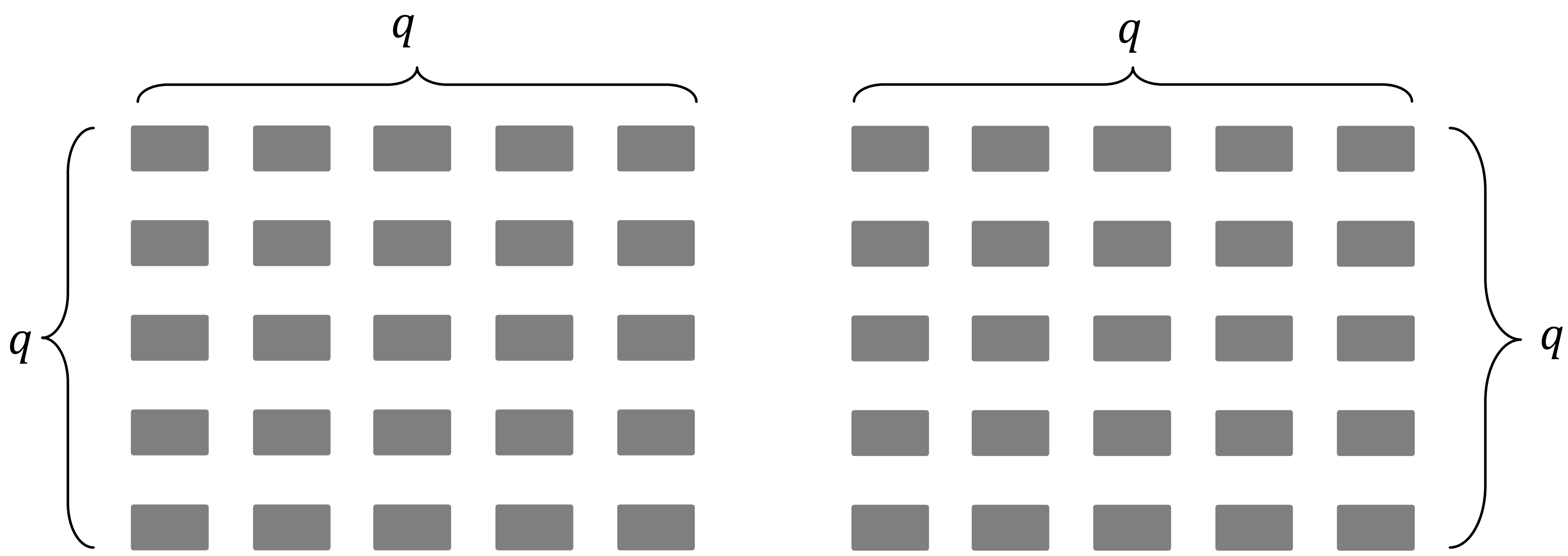

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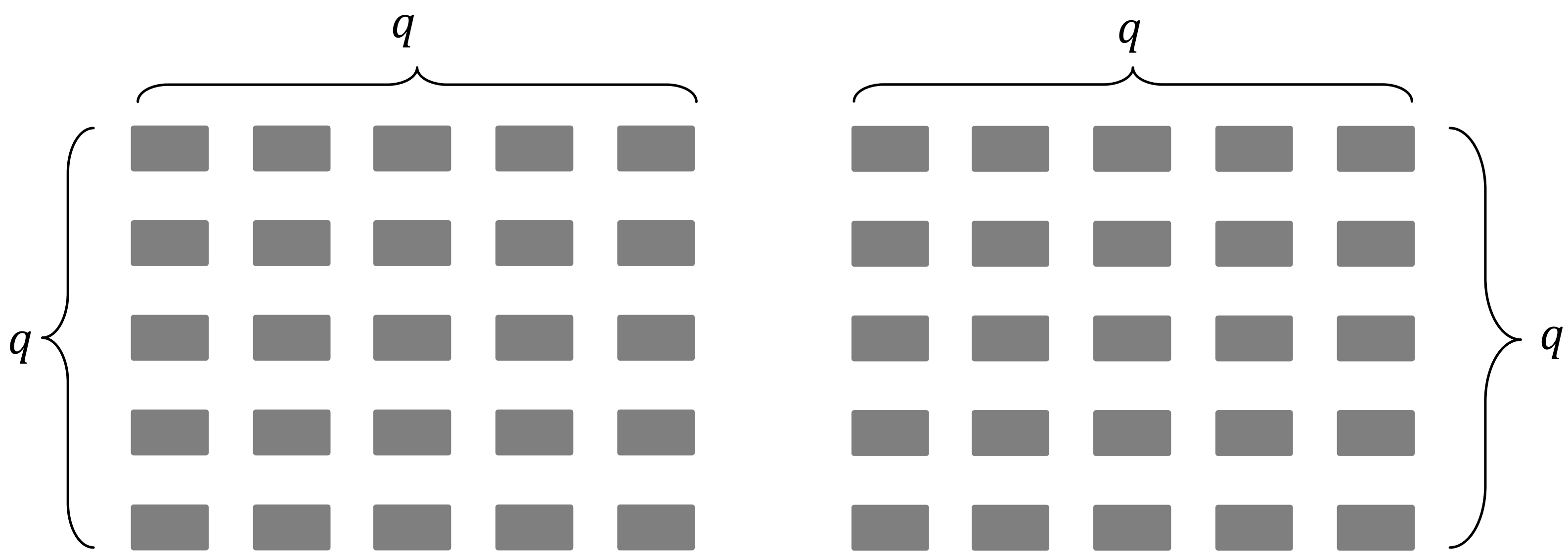

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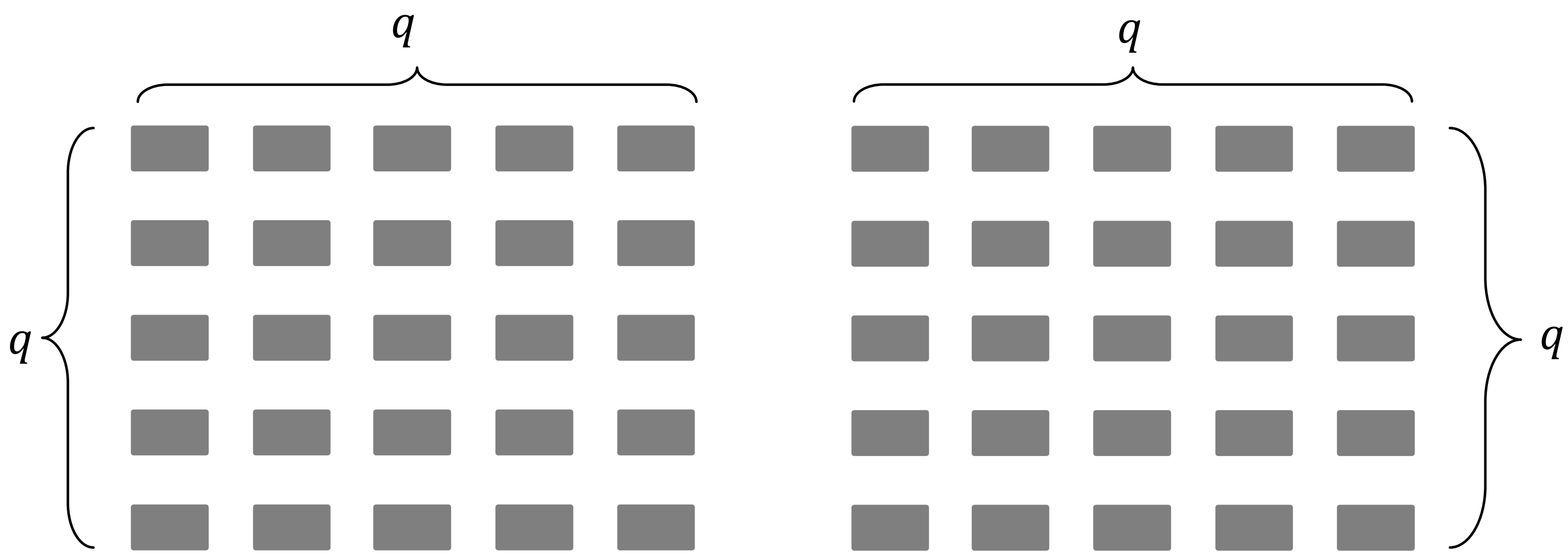

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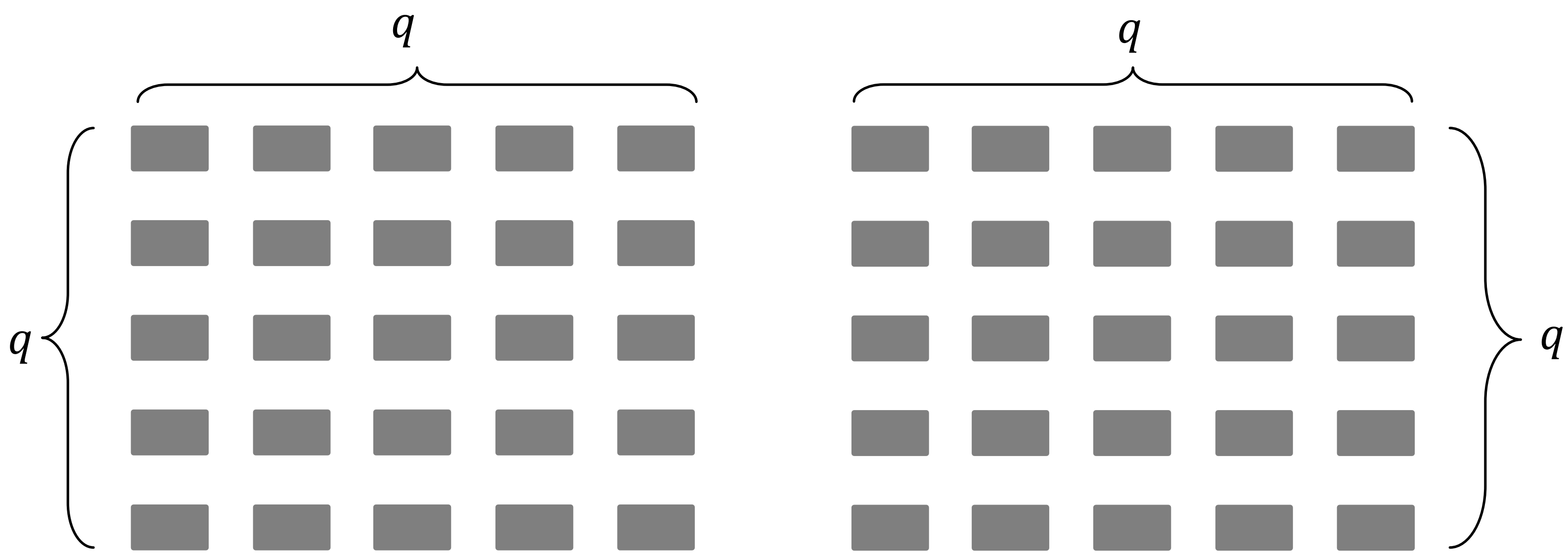

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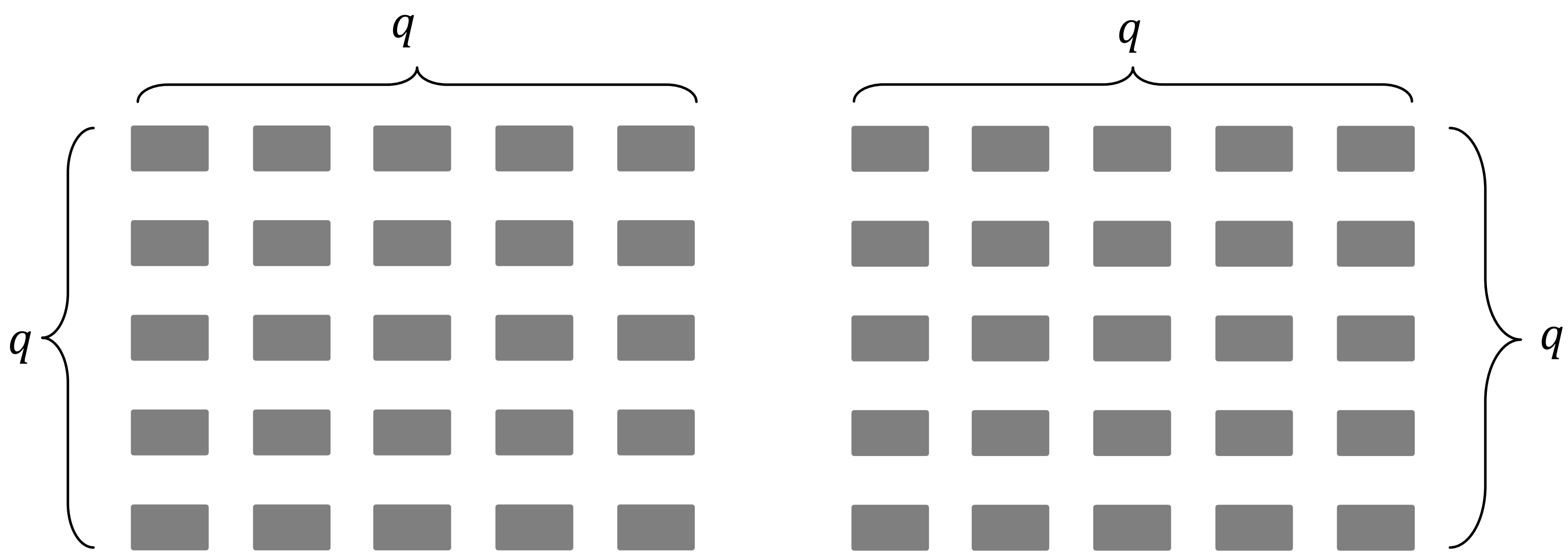

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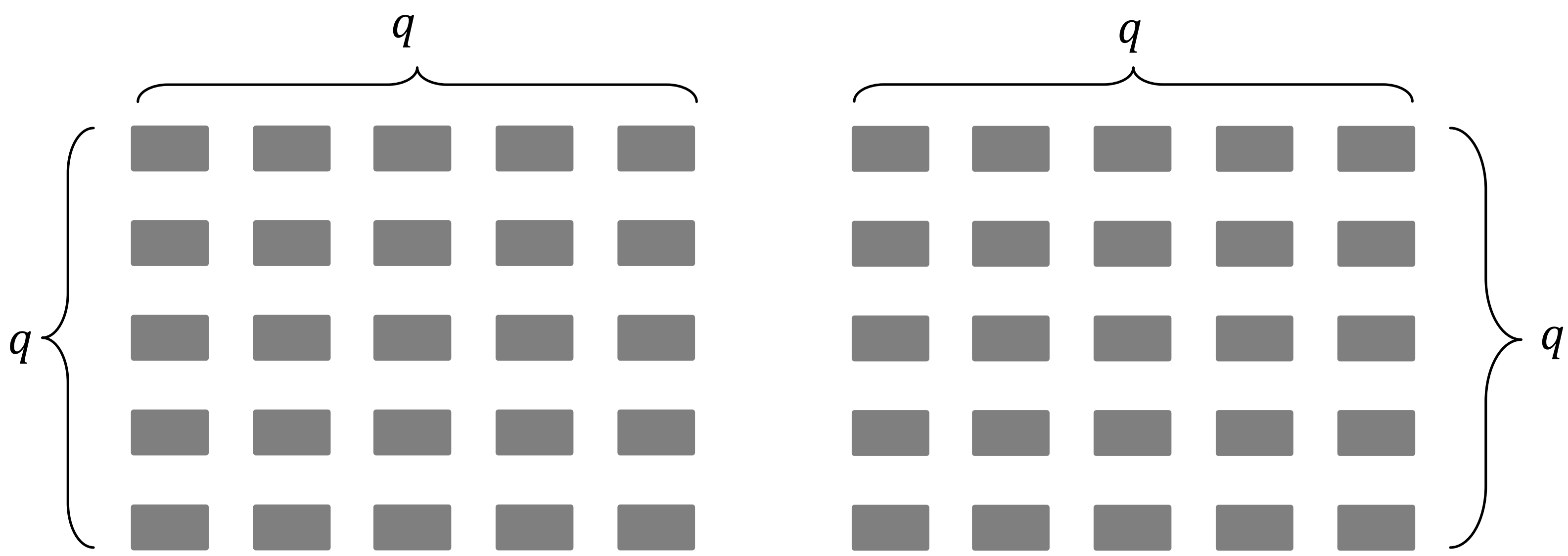
E *Example*: $q = 5$



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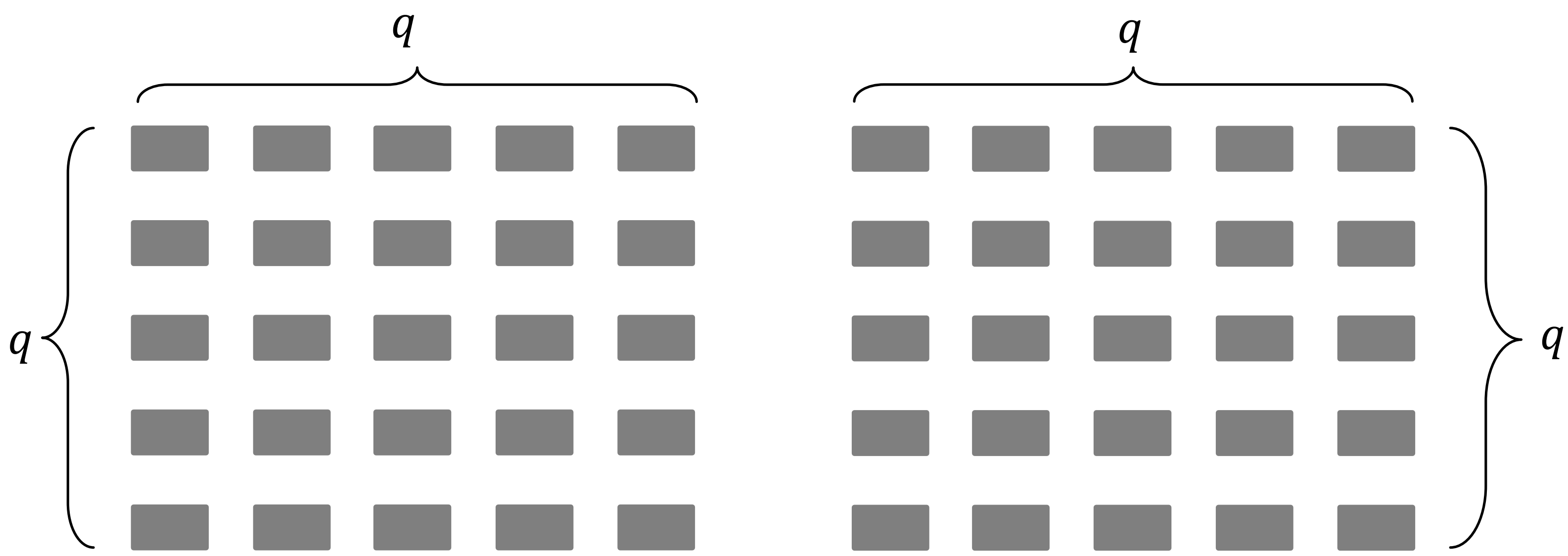
50 routers
network radix: 7



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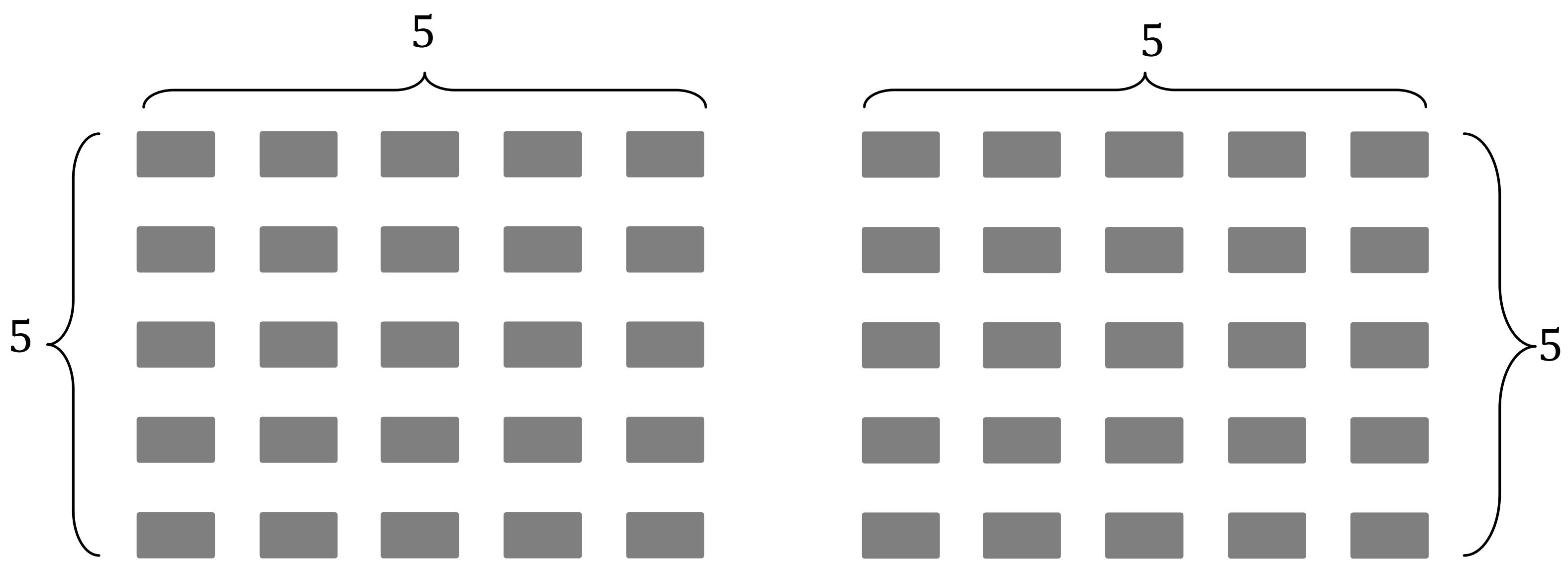

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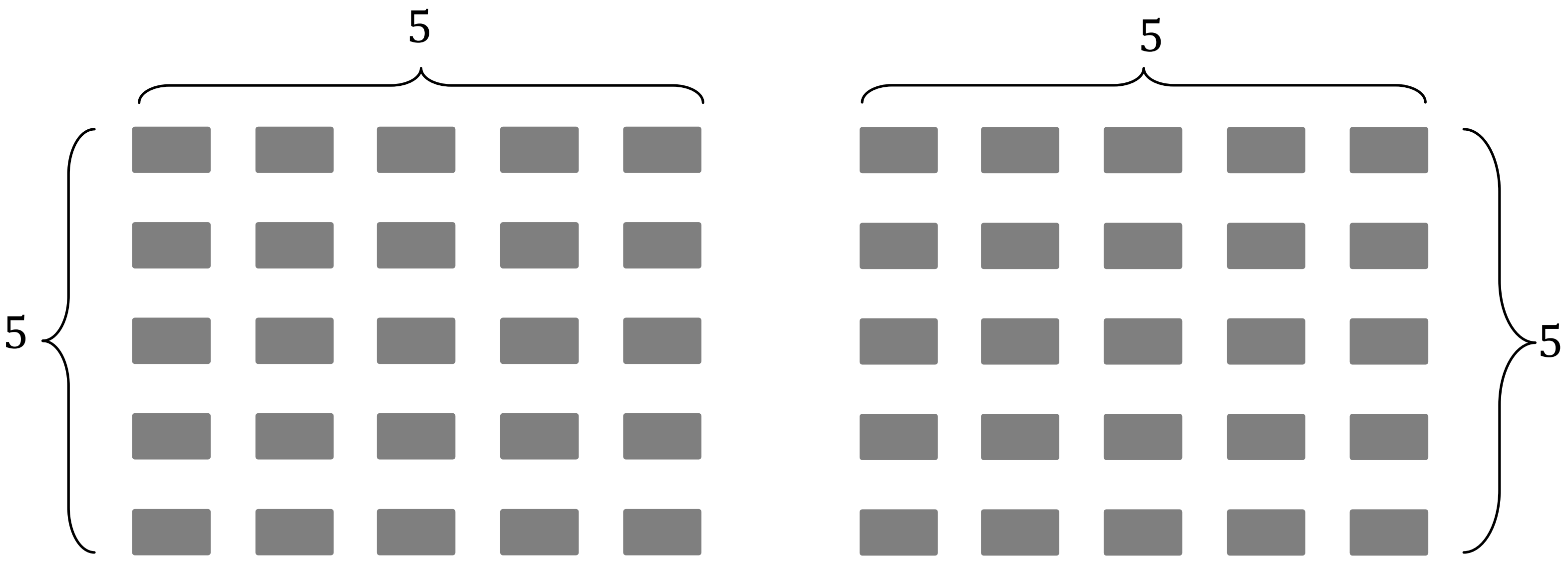
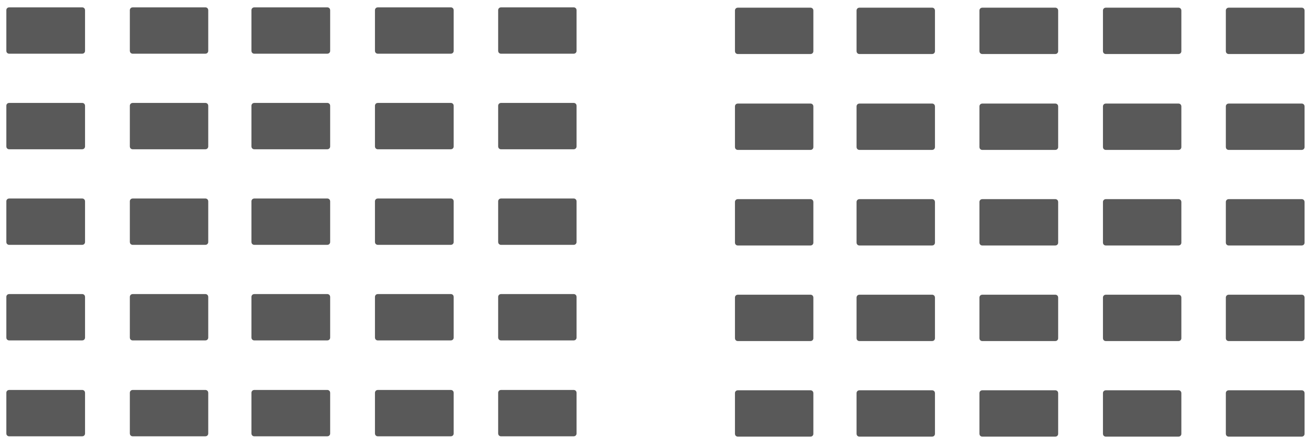
network radix: 7

$$\mathcal{F}_5 = \{0,1,2,3,4\}$$

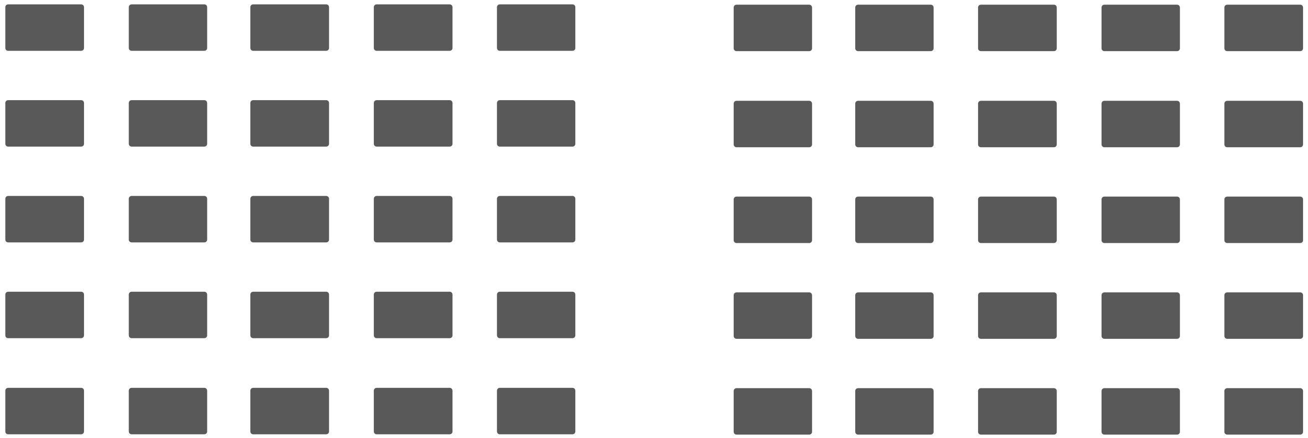


Diameter-2 Slim Fly



Diameter-2 Slim Fly

3 *Label the routers*



Diameter-2 Slim Fly

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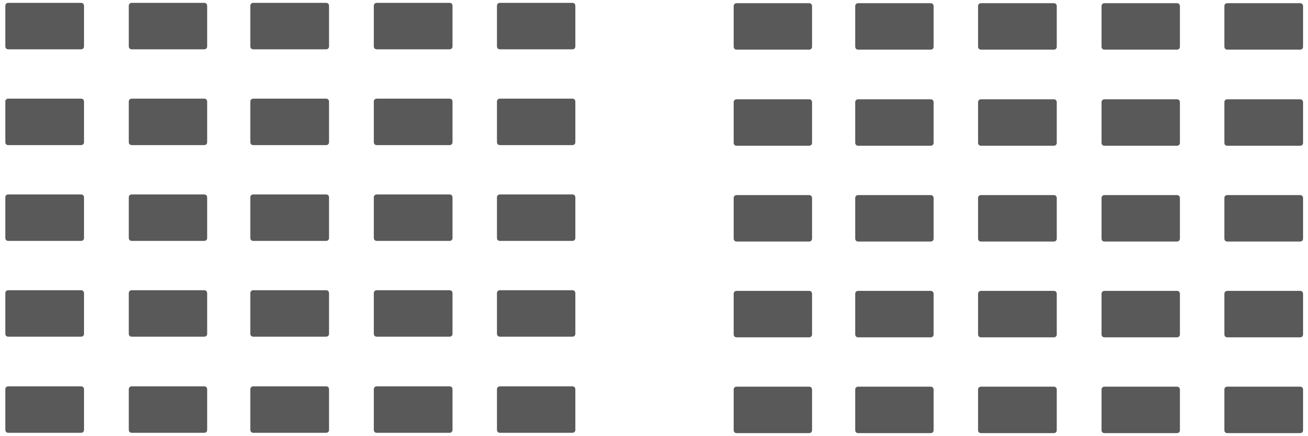
Set of routers:

$$\{0,1\} \times \mathcal{F}_q \times \mathcal{F}_q$$



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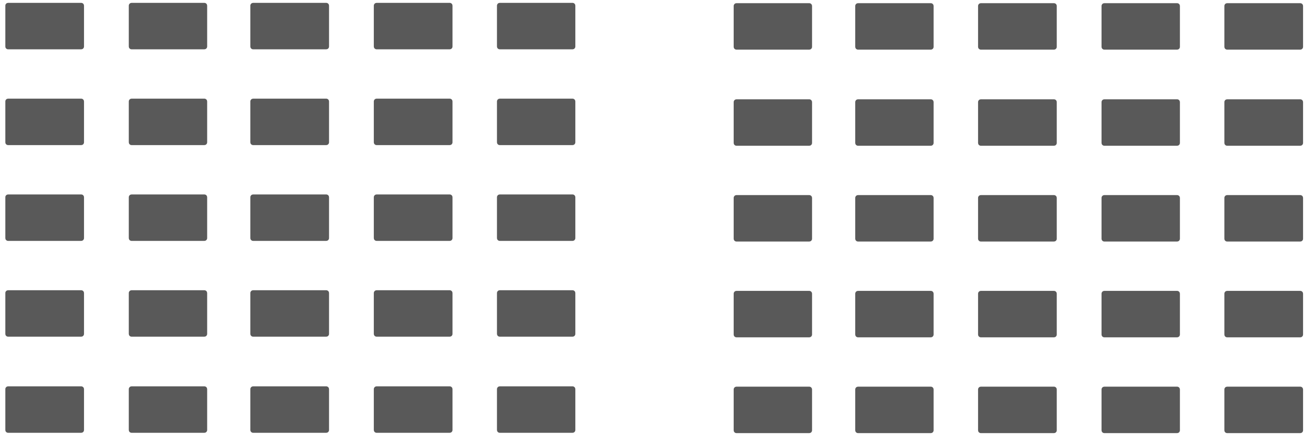

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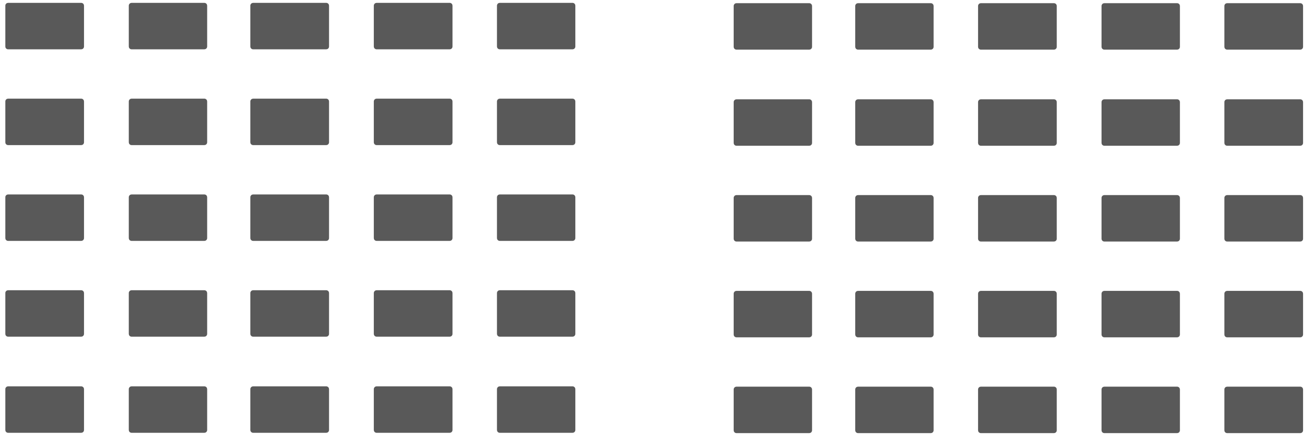

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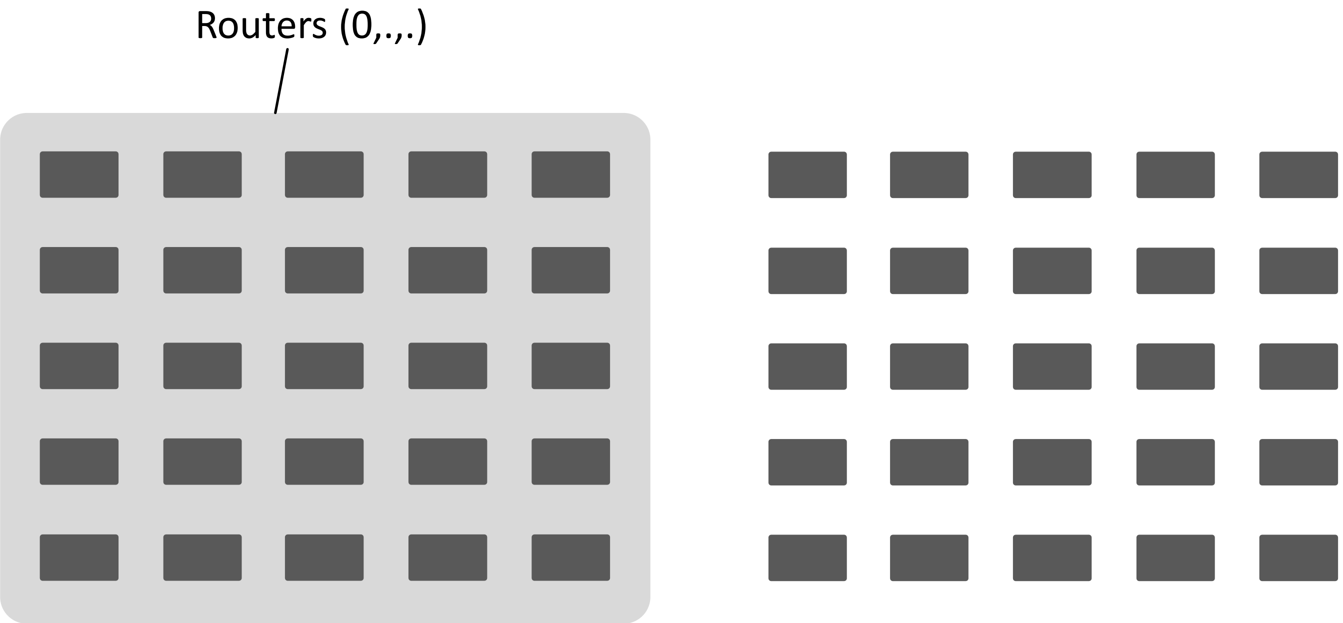

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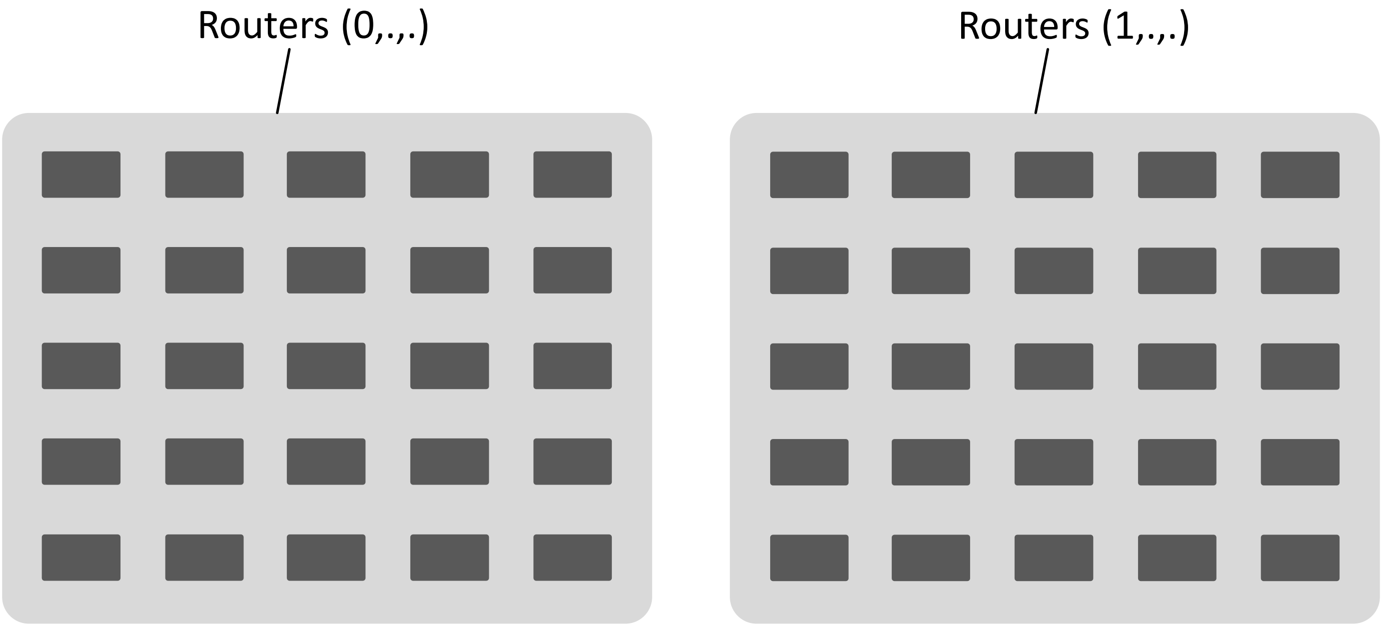

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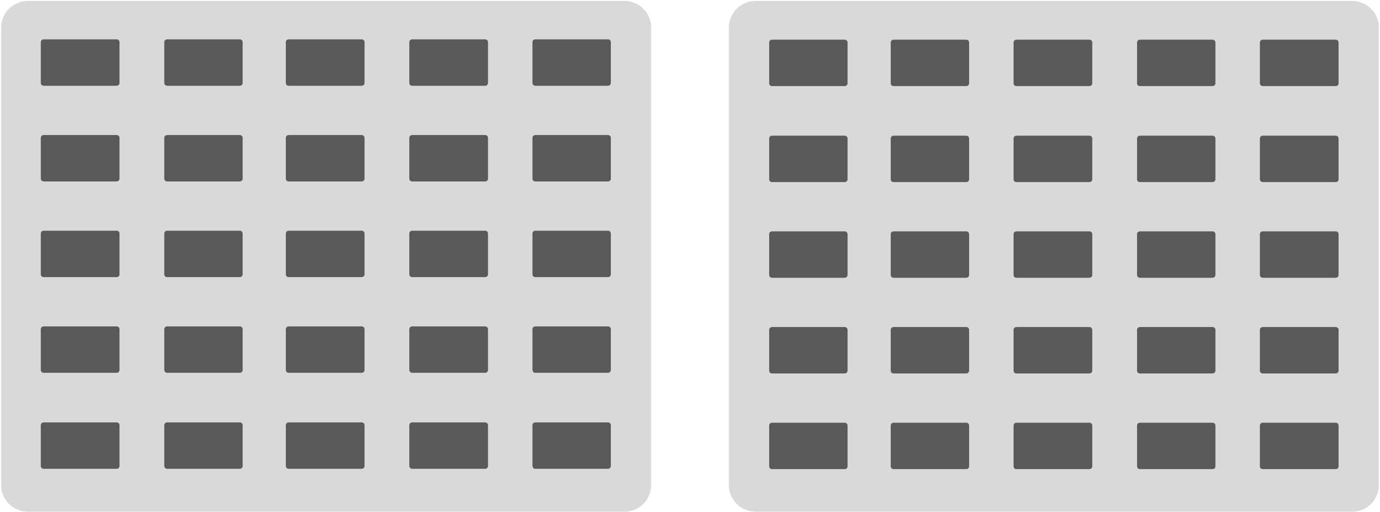

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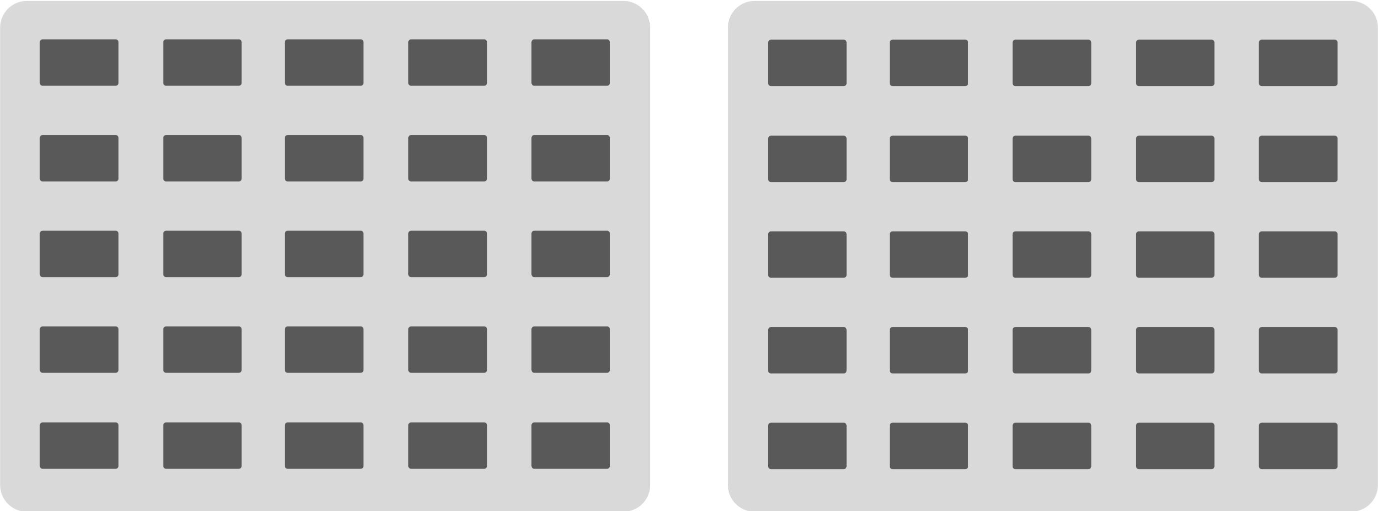

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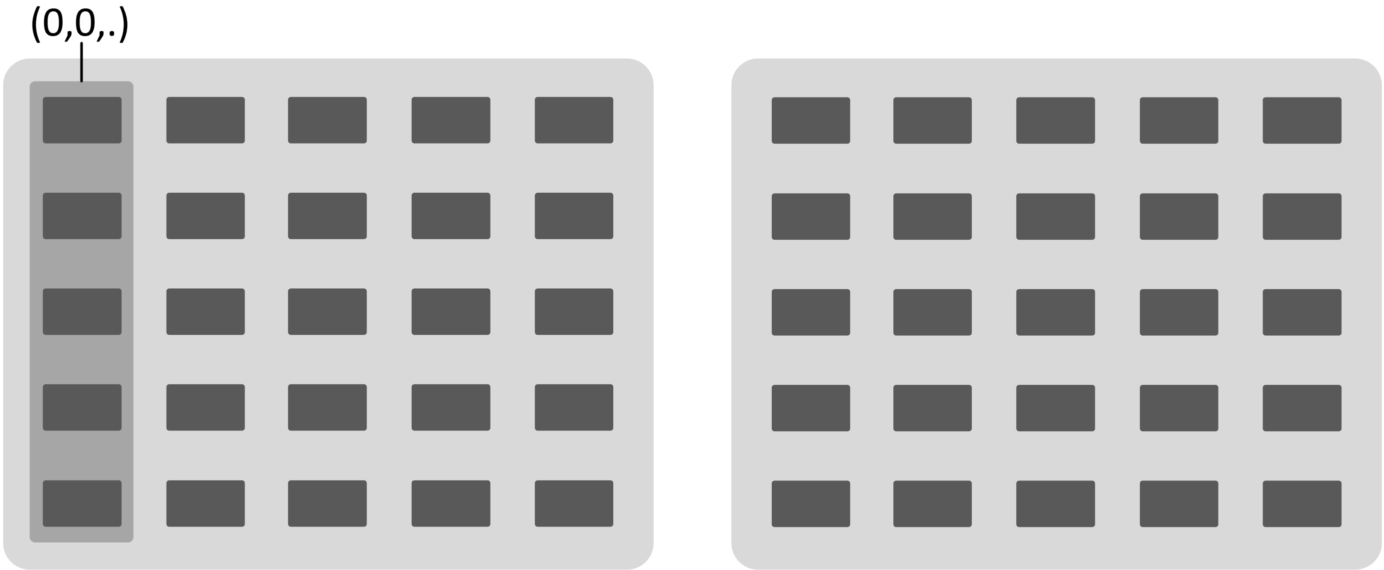

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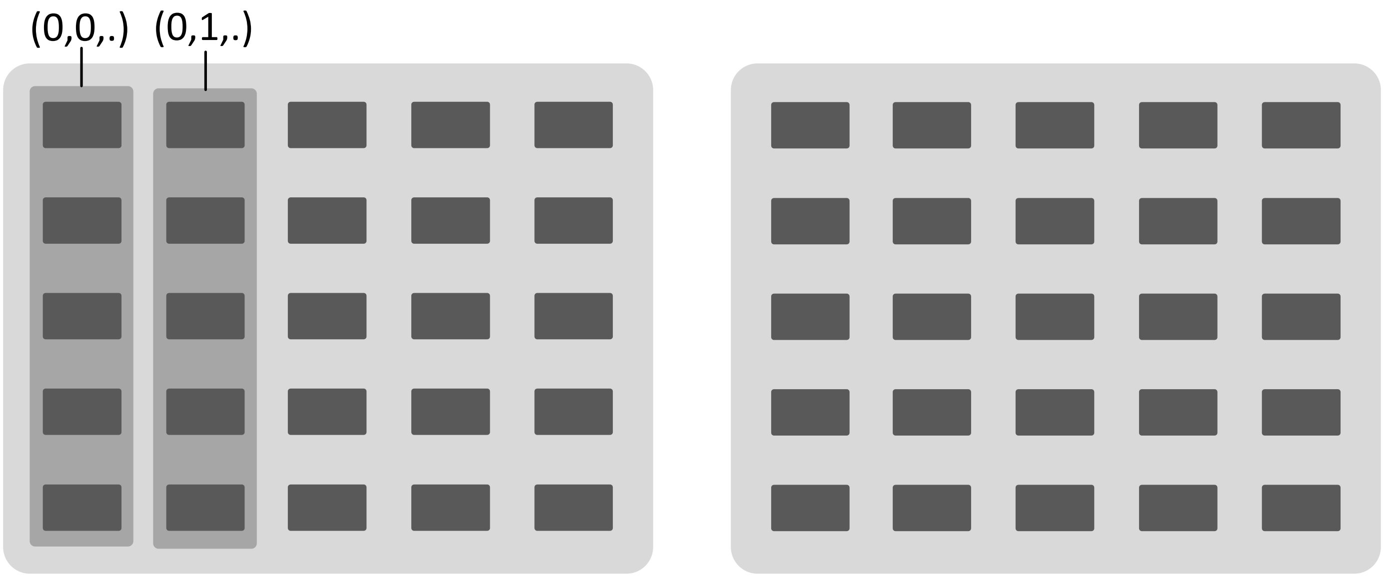

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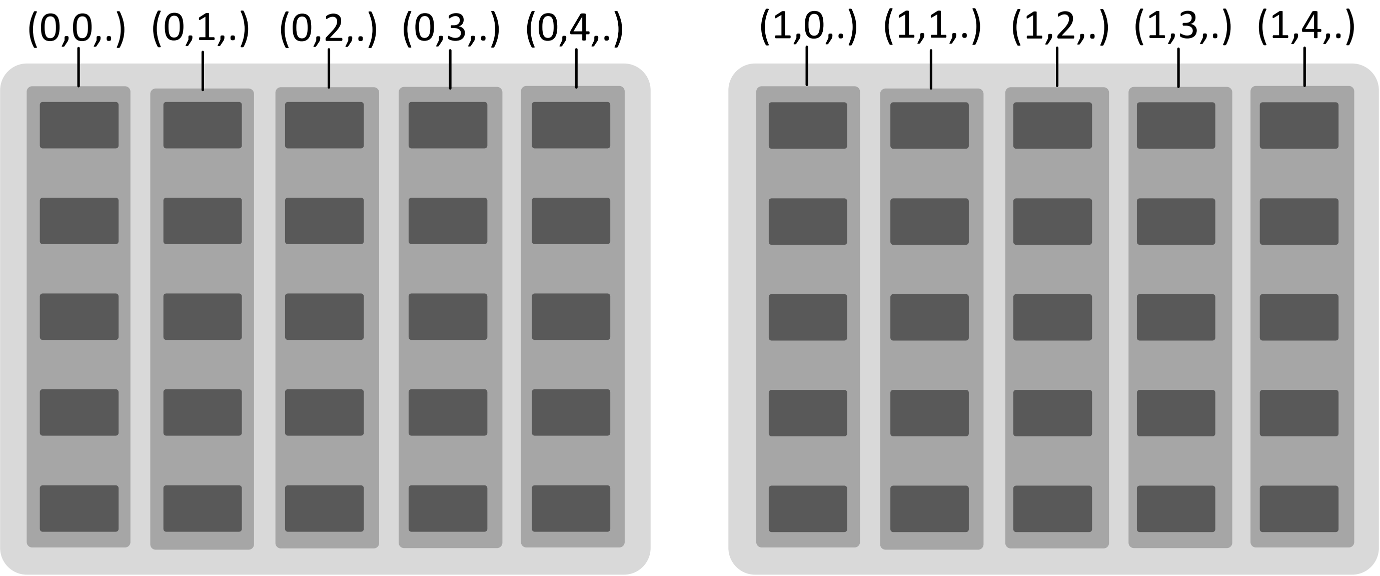

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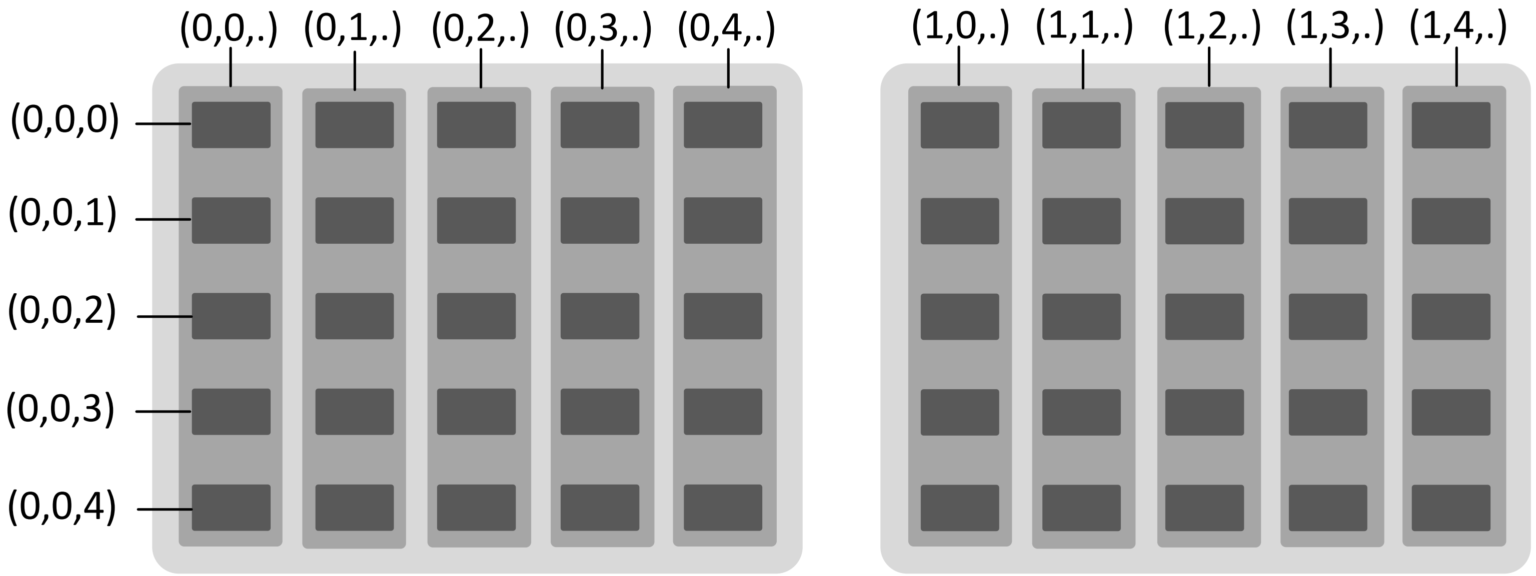

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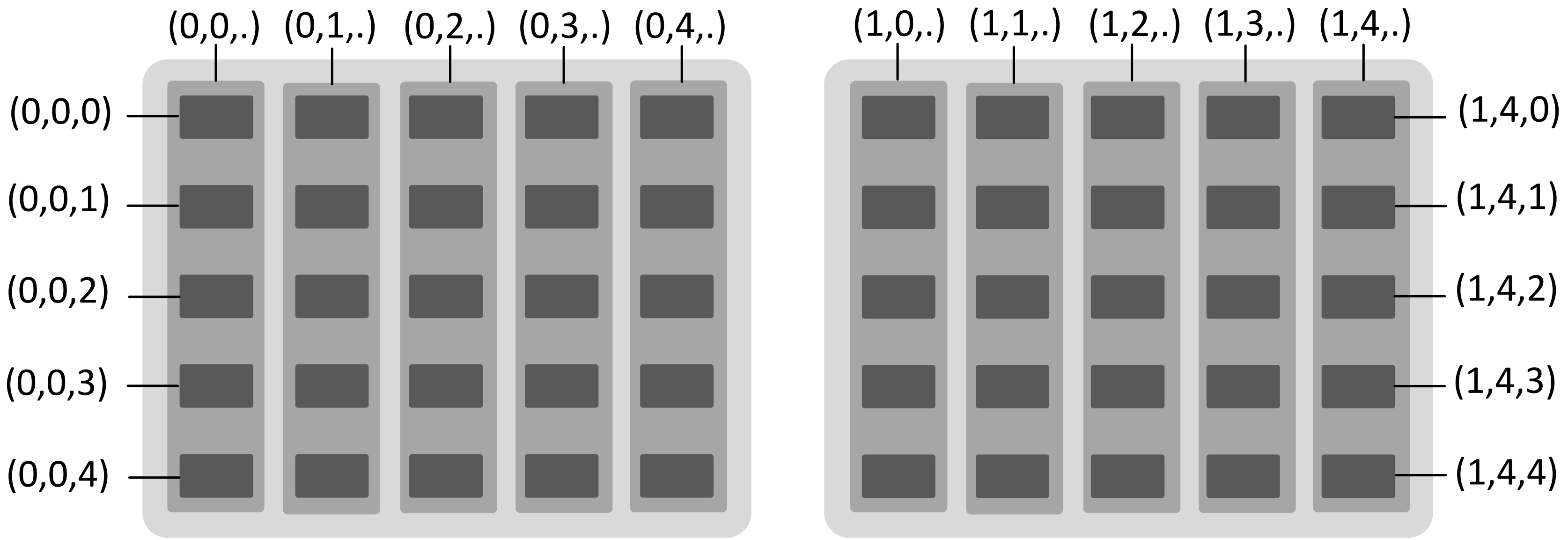
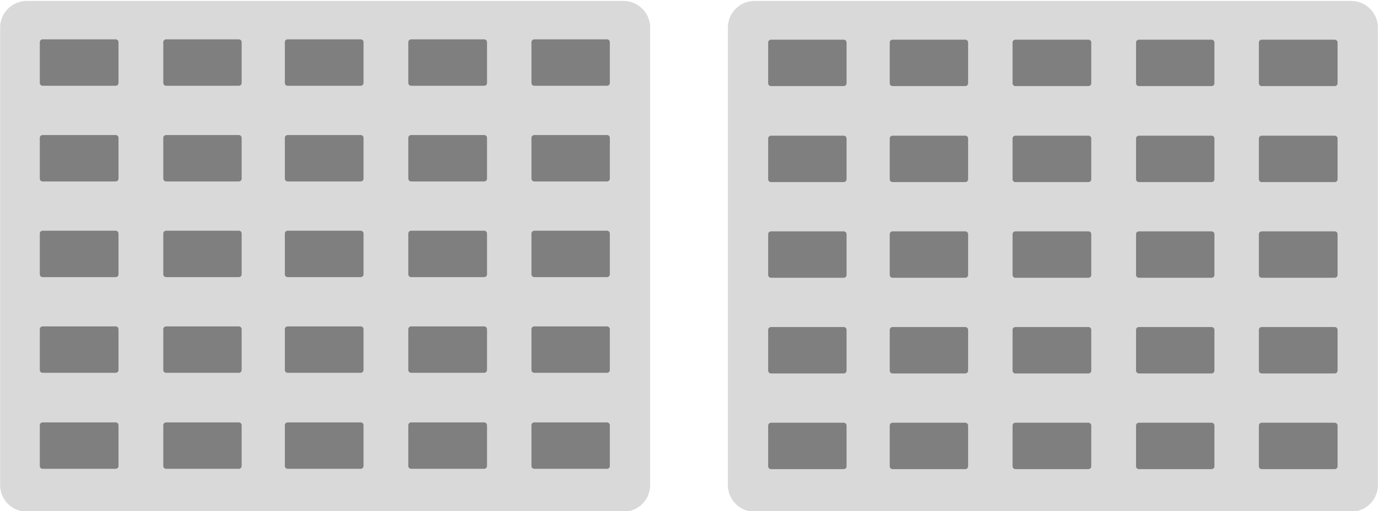


Diameter-2 Slim Fly

4 *Find primitive element* ξ



Diameter-2 Slim Fly

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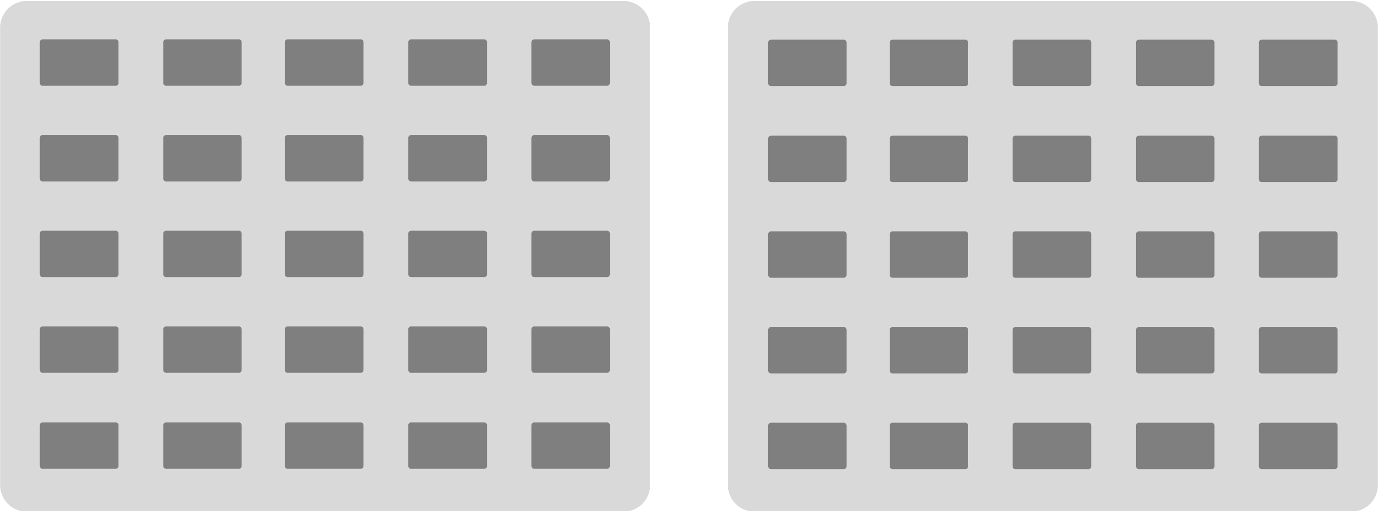
$\xi \in \mathcal{F}_q$ generates $\mathcal{F}_q$



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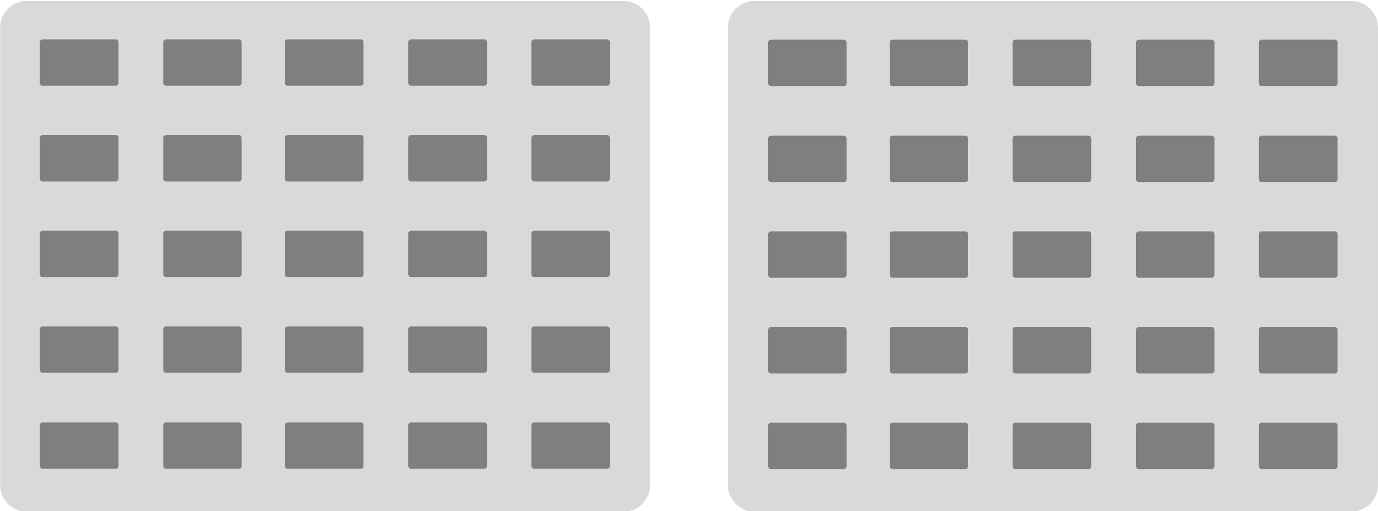

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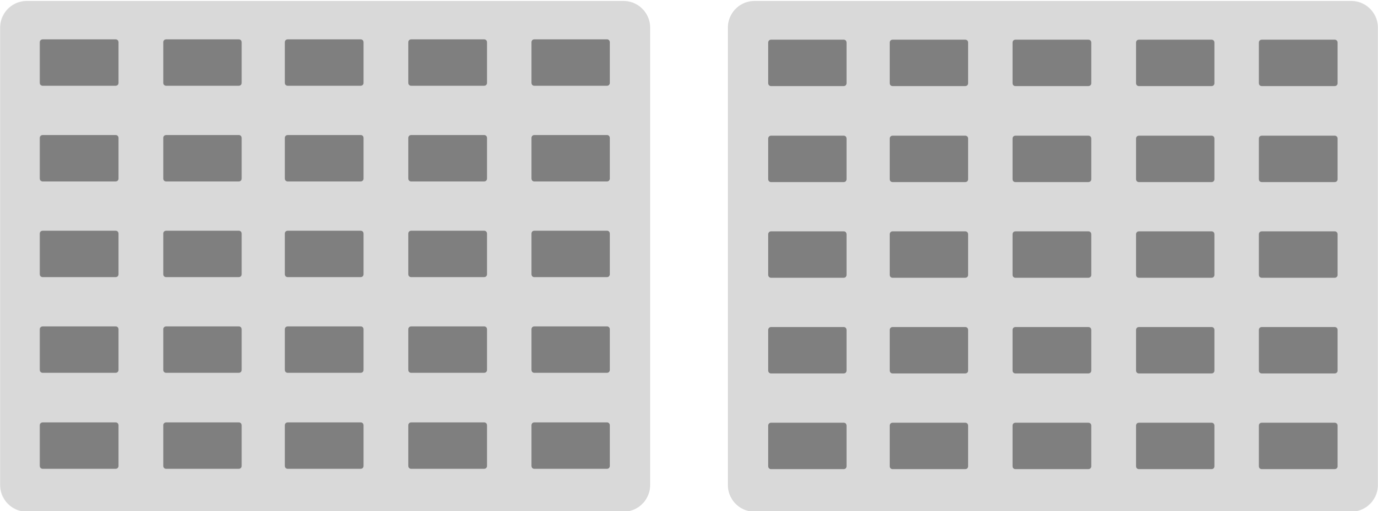

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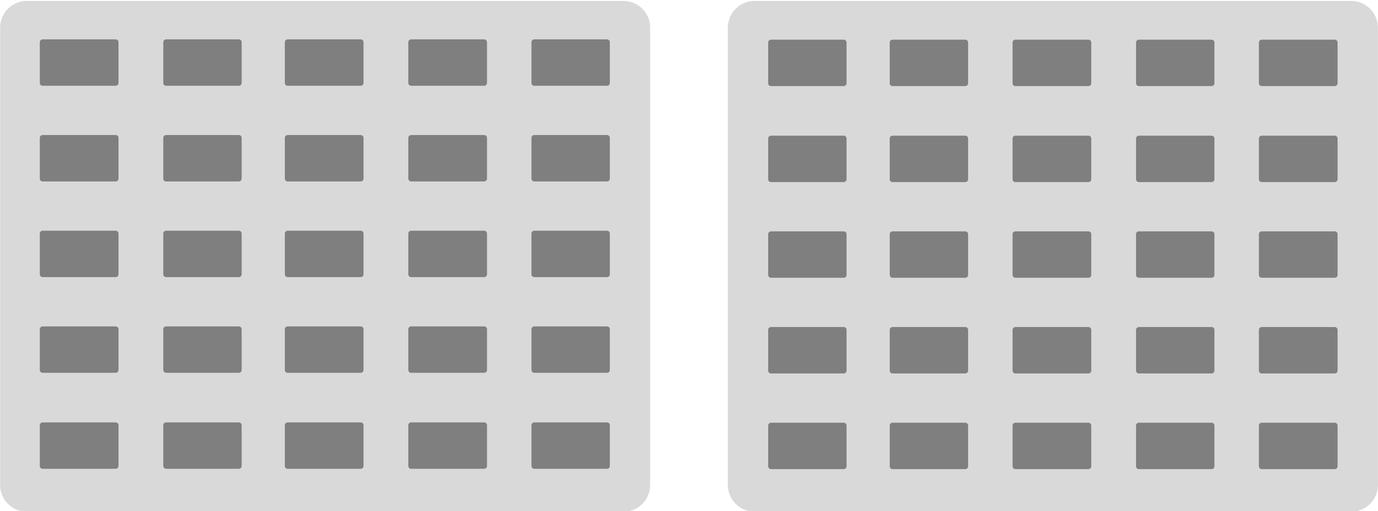

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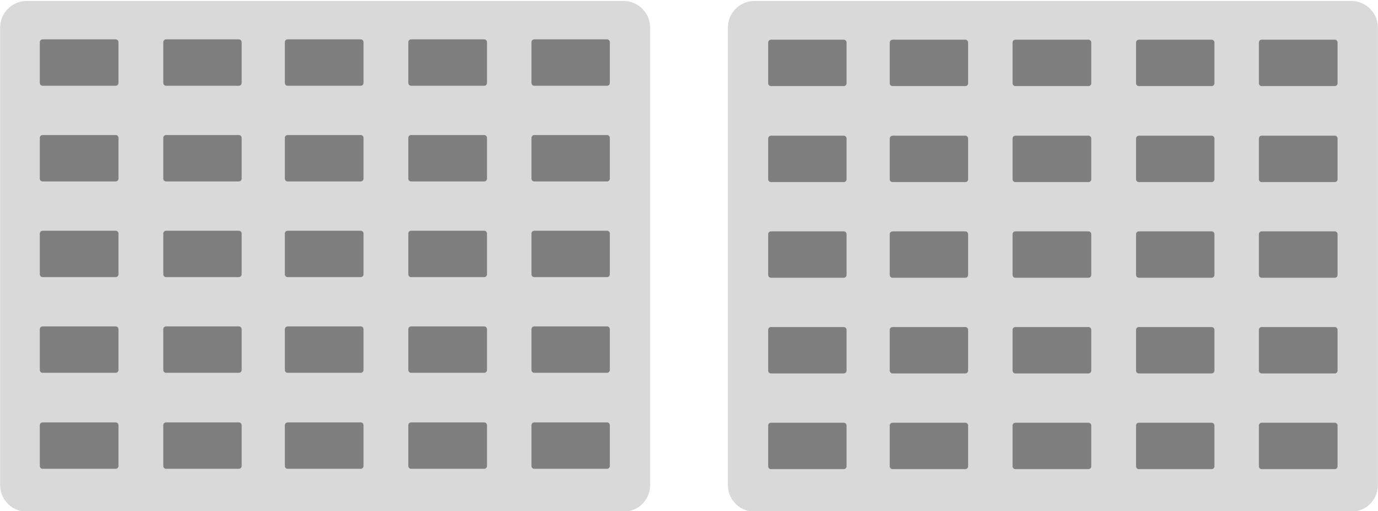
$\mathcal{F}_5 = \{0,1,2,3,4\}$

$\xi = 2$



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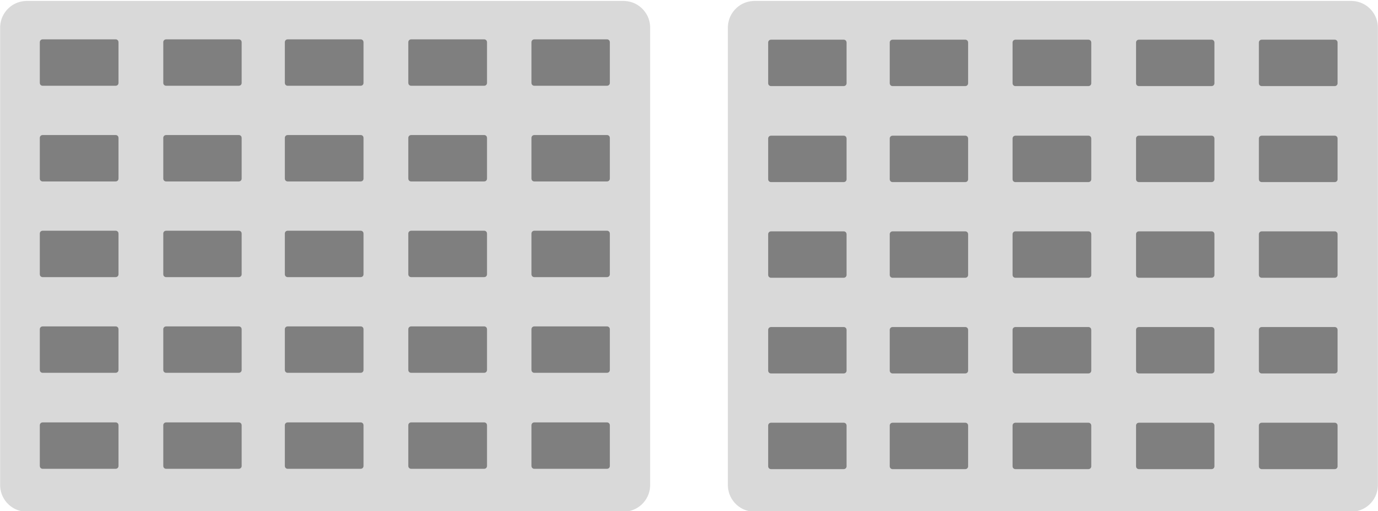
$\mathcal{F}_5 = \{0,1,2,3,4\}$

$\xi = 2$

$1 = \xi^4 \mod 5 = 2^4 \mod 5 = 16 \mod 5$



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$$X = \{1, \xi^2, \ldots, \xi^{q-3}\}$$

$$X' = \{\xi, \xi^3, \ldots, \xi^{q-2}\}$$

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$$\mathcal{F}_5 = \{0,1,2,3,4\}$$

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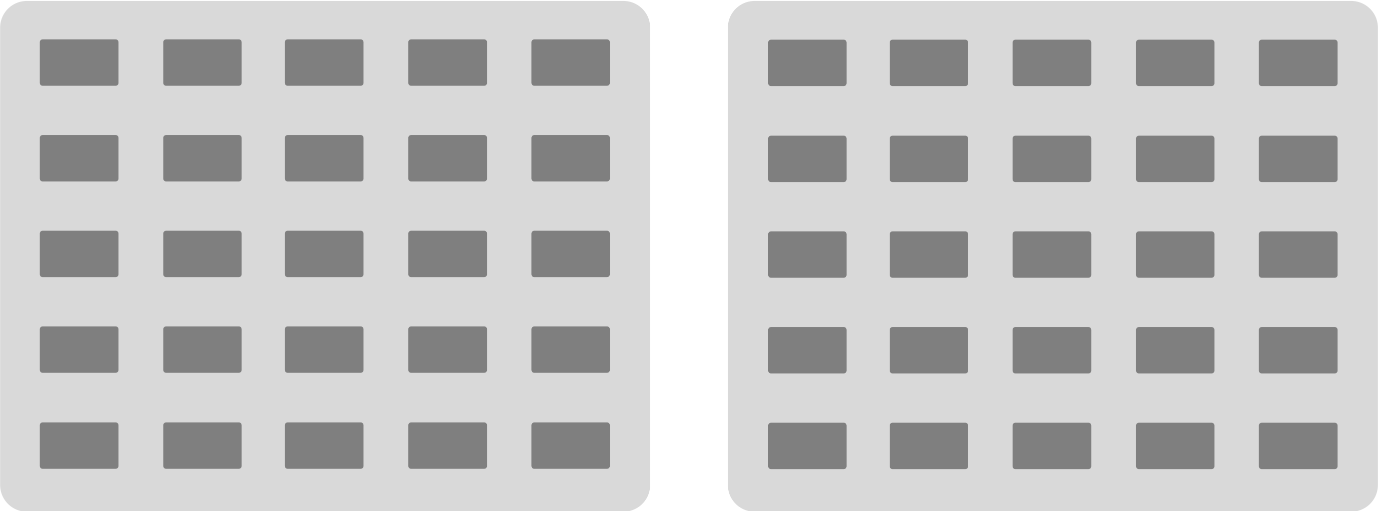

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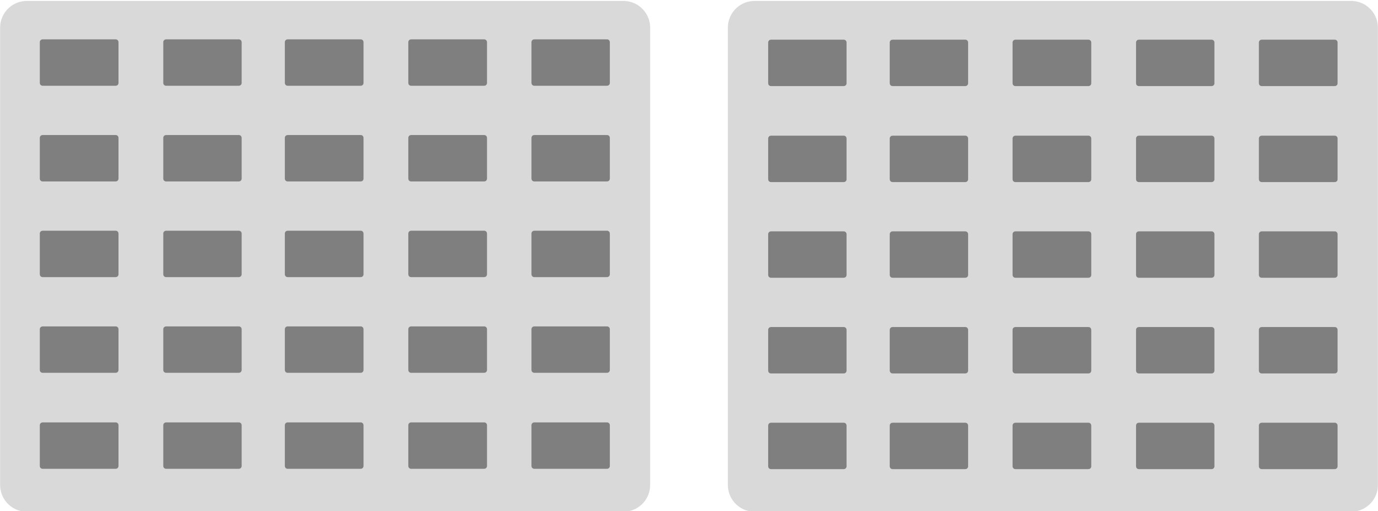

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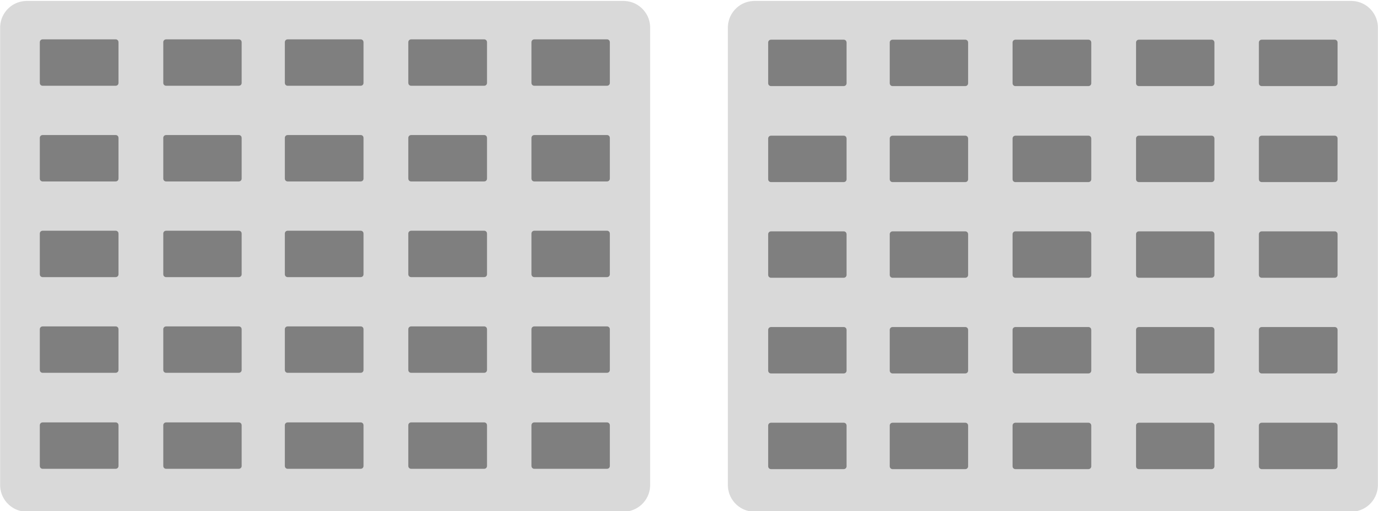
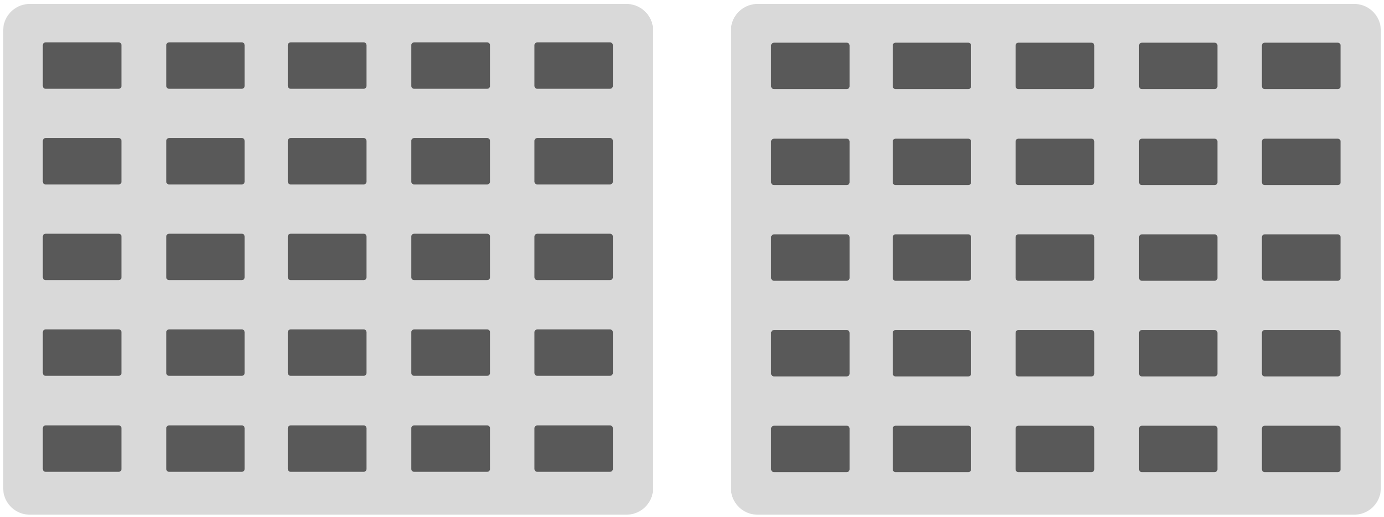
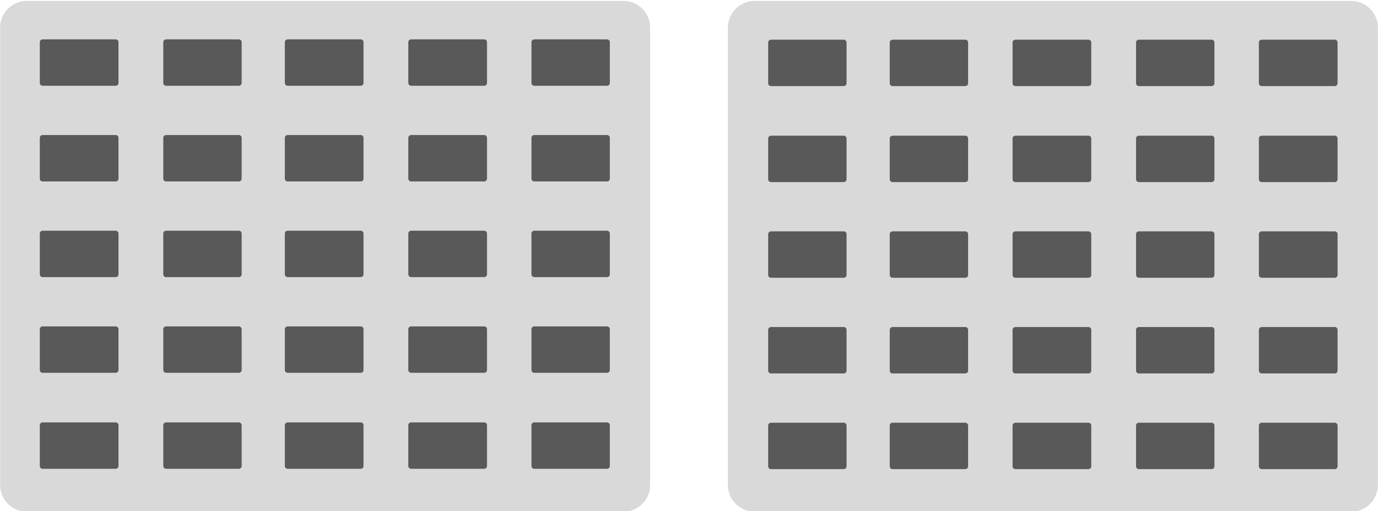


DIAMETER-2 SLIM FLY



Diameter-2 Slim Fly

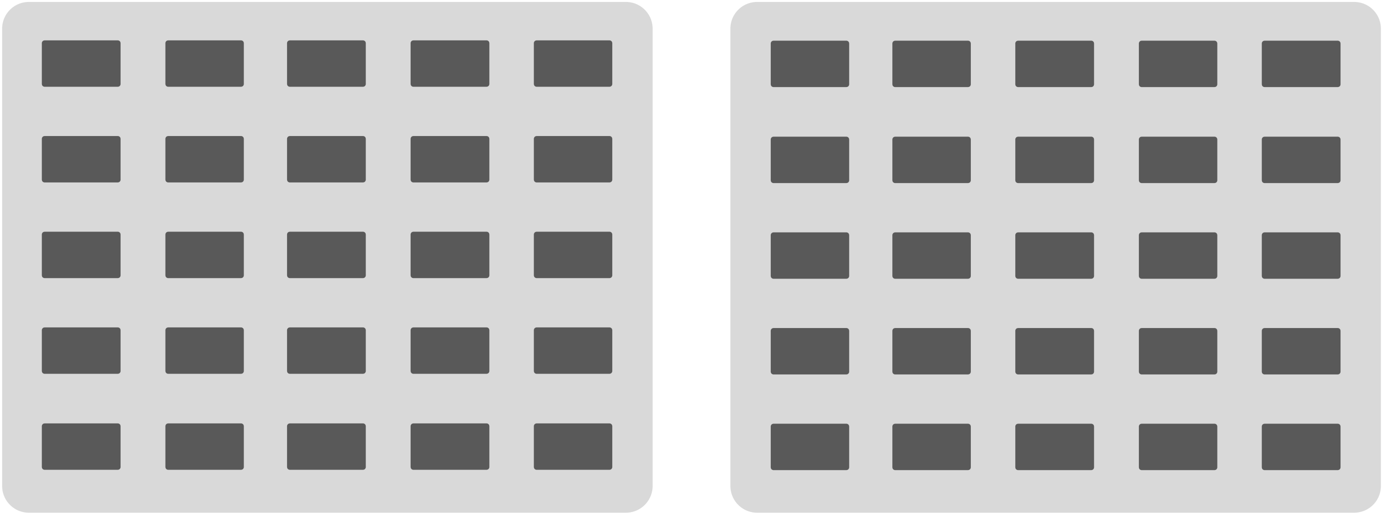
6 *Intra-group connections*



Diameter-2 Slim Fly

6 *Intra-group connections*

Two routers in one group are connected iff their "vertical Manhattan distance" is an element from:



Diameter-2 Slim Fly

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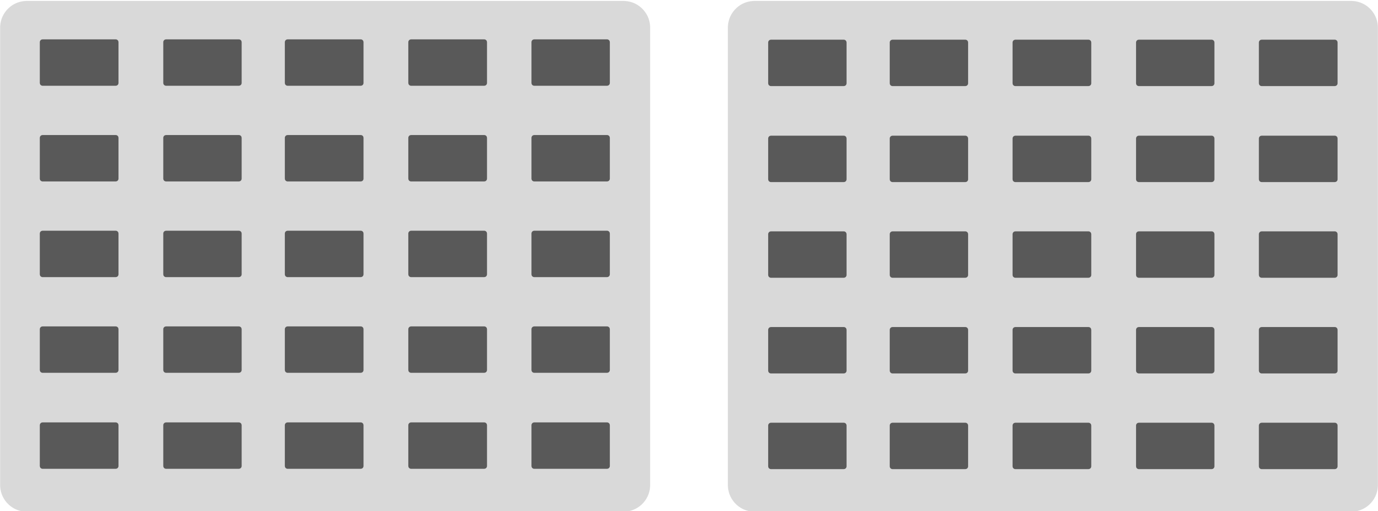
Two routers in one group are connected iff their "vertical Manhattan distance" is an element from:

$$X = \{1, \xi^2, \ldots, \xi^{q-3}\}$$ (for subgraph 0)



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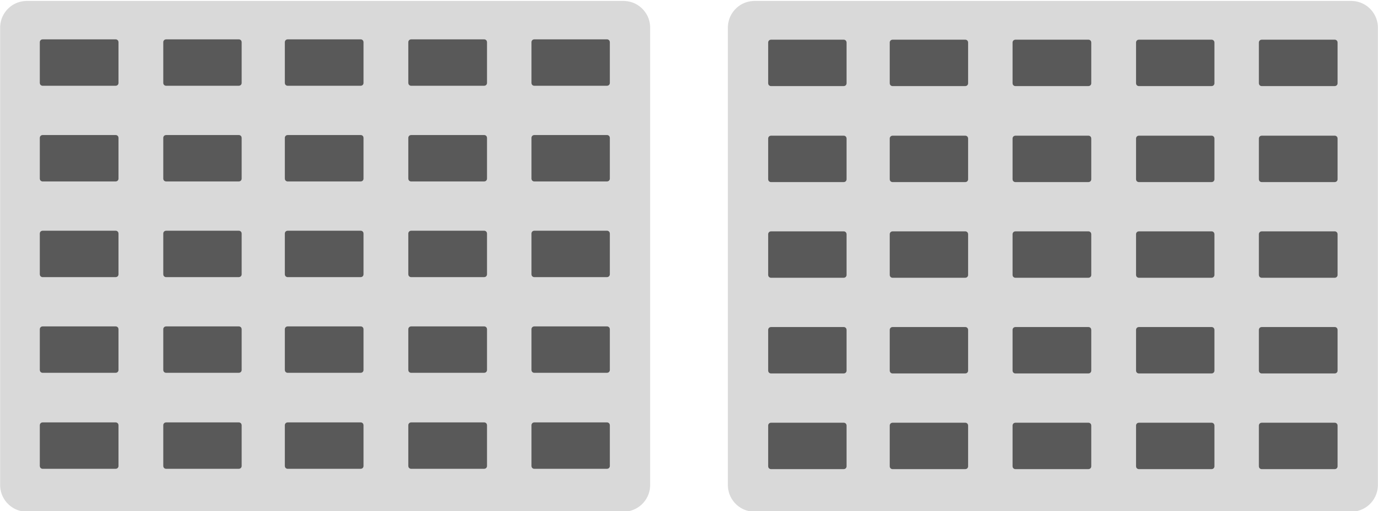

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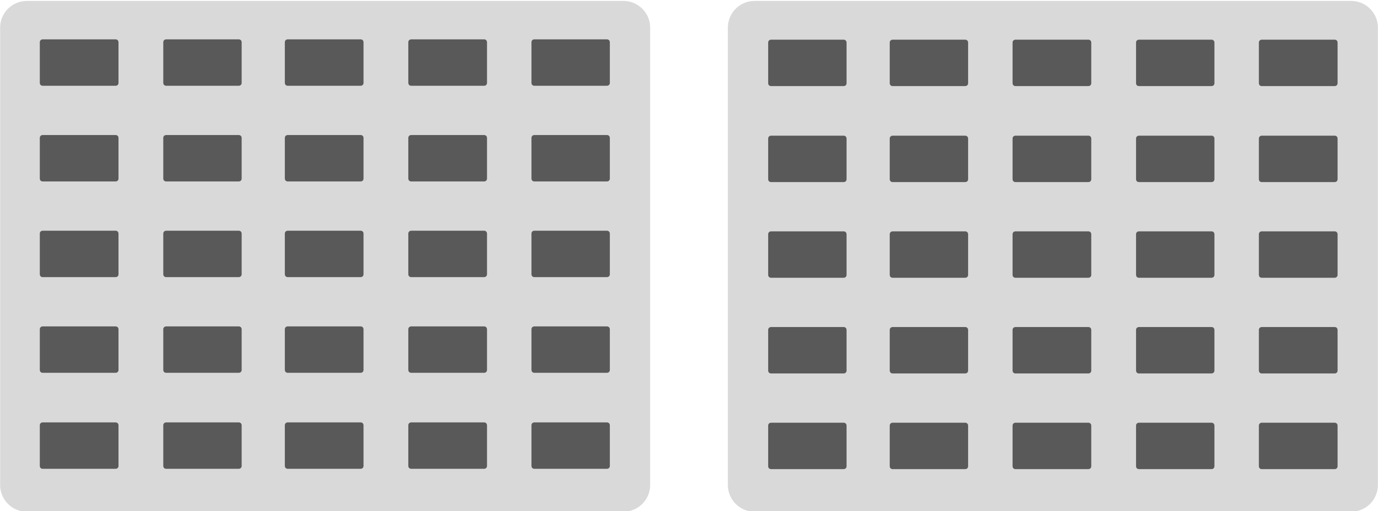
E *Example:* $q = 5$

Take Routers $(0,0,.)$



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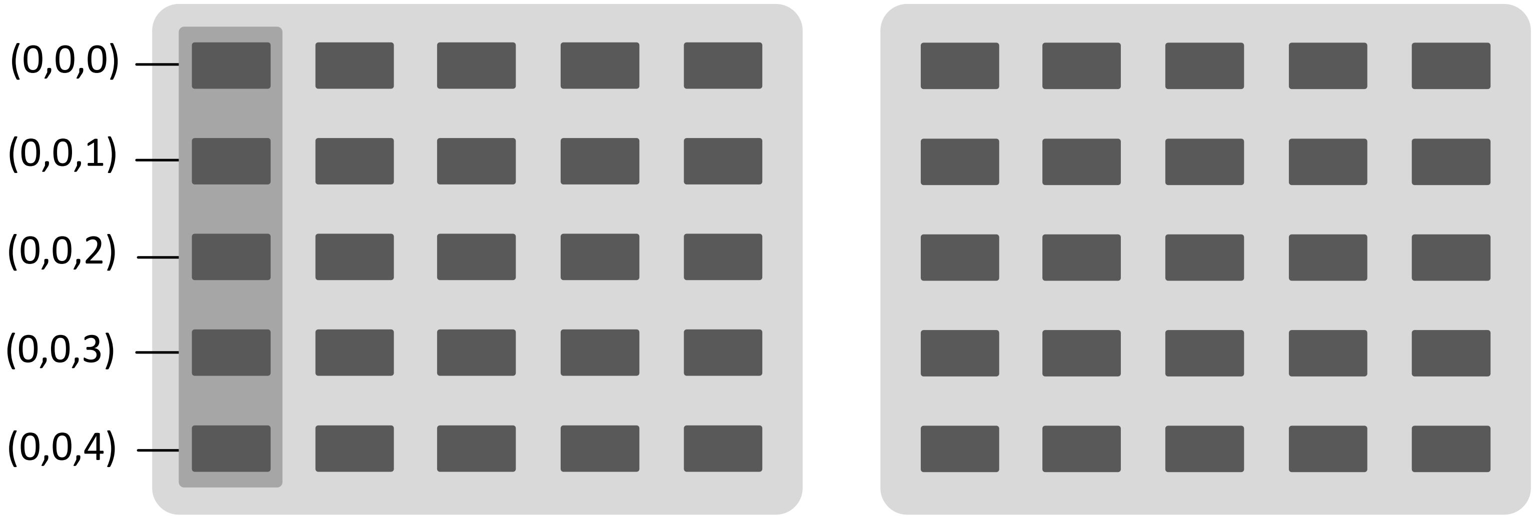

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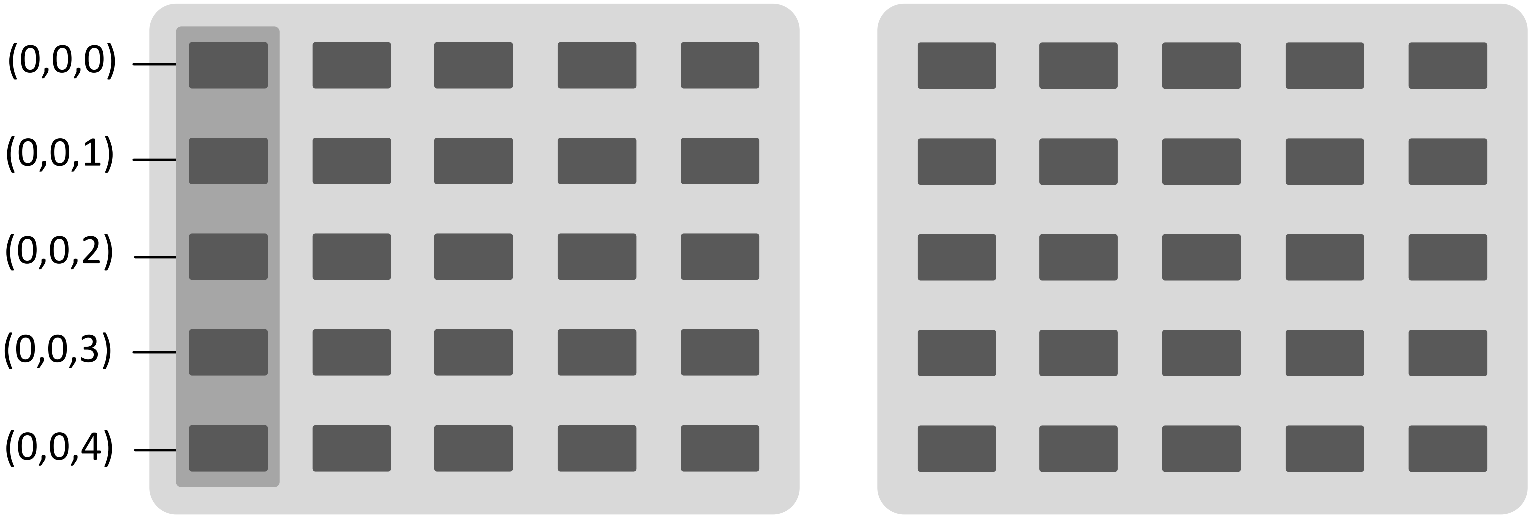

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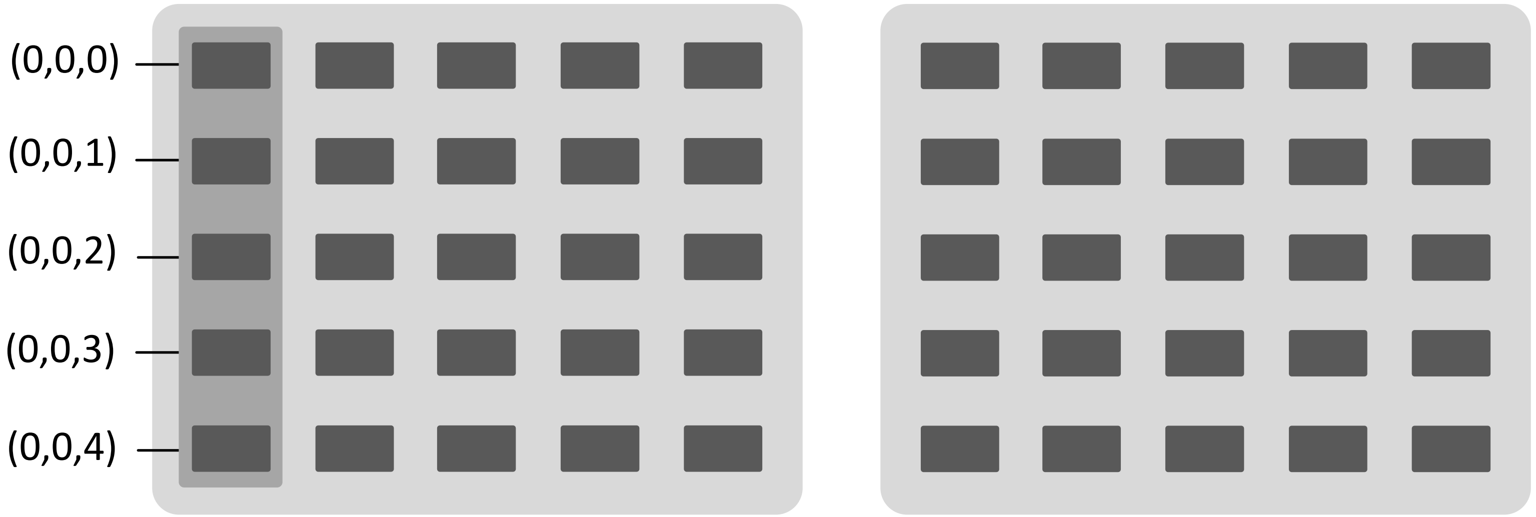

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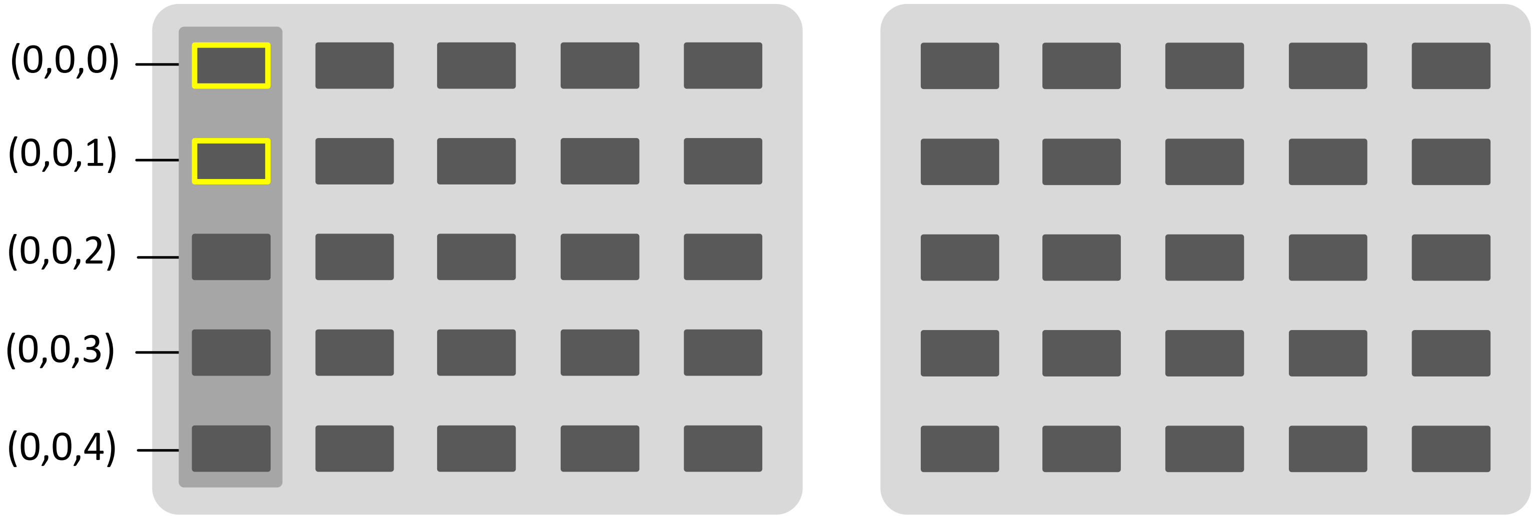

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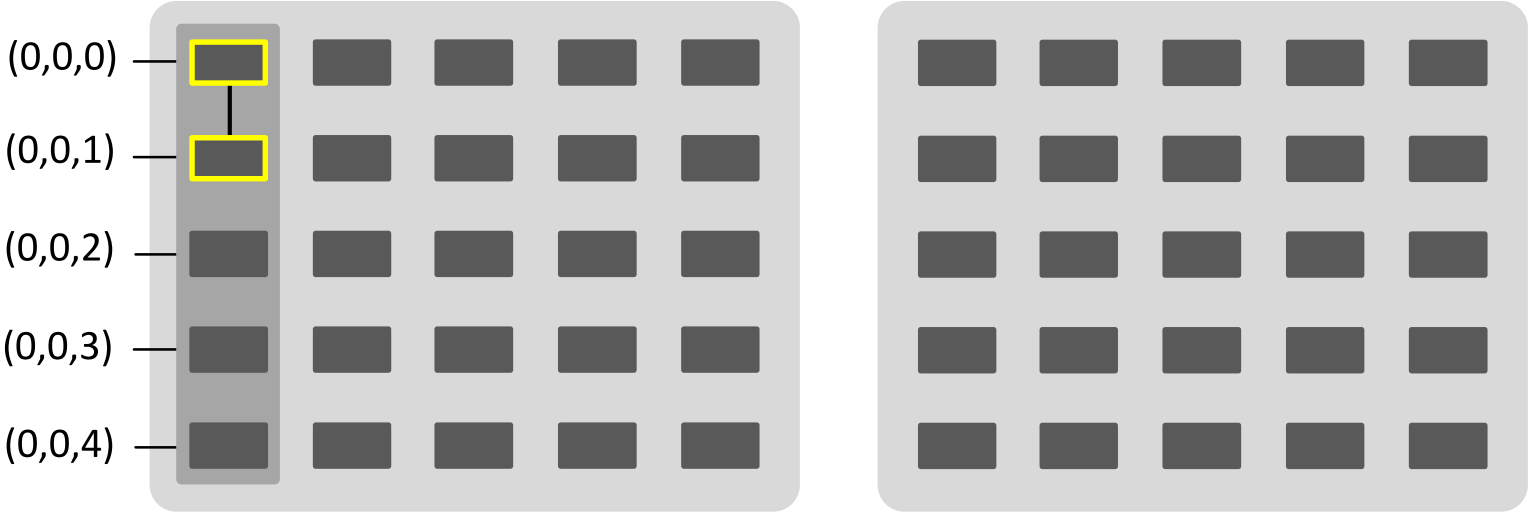

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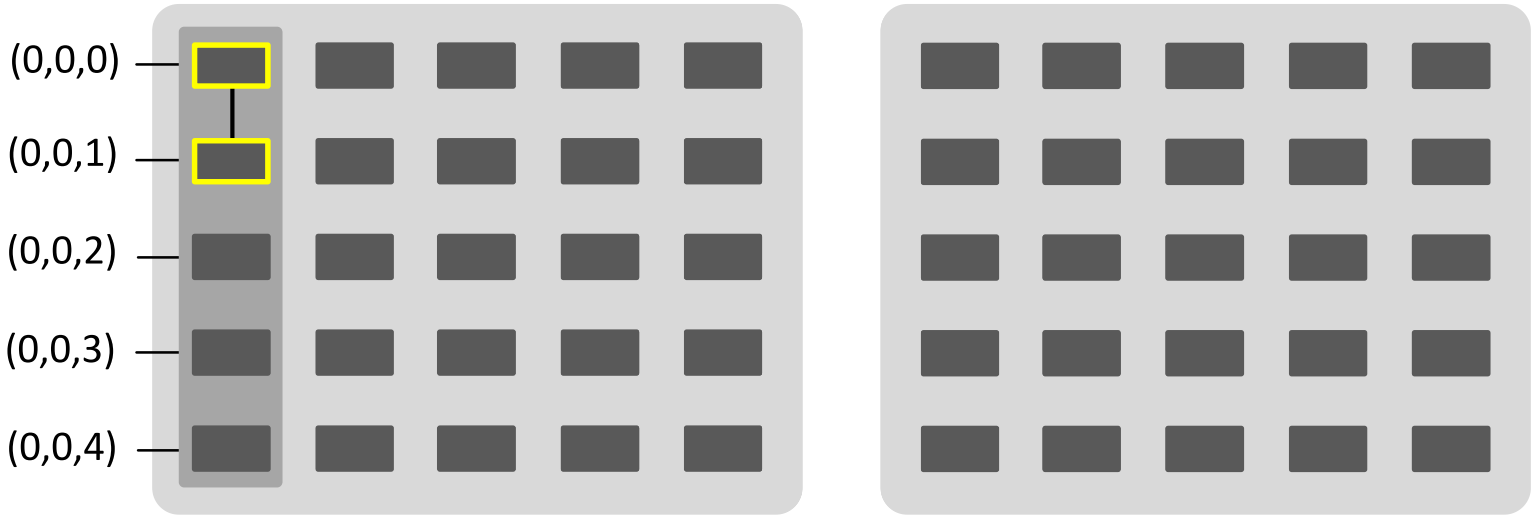

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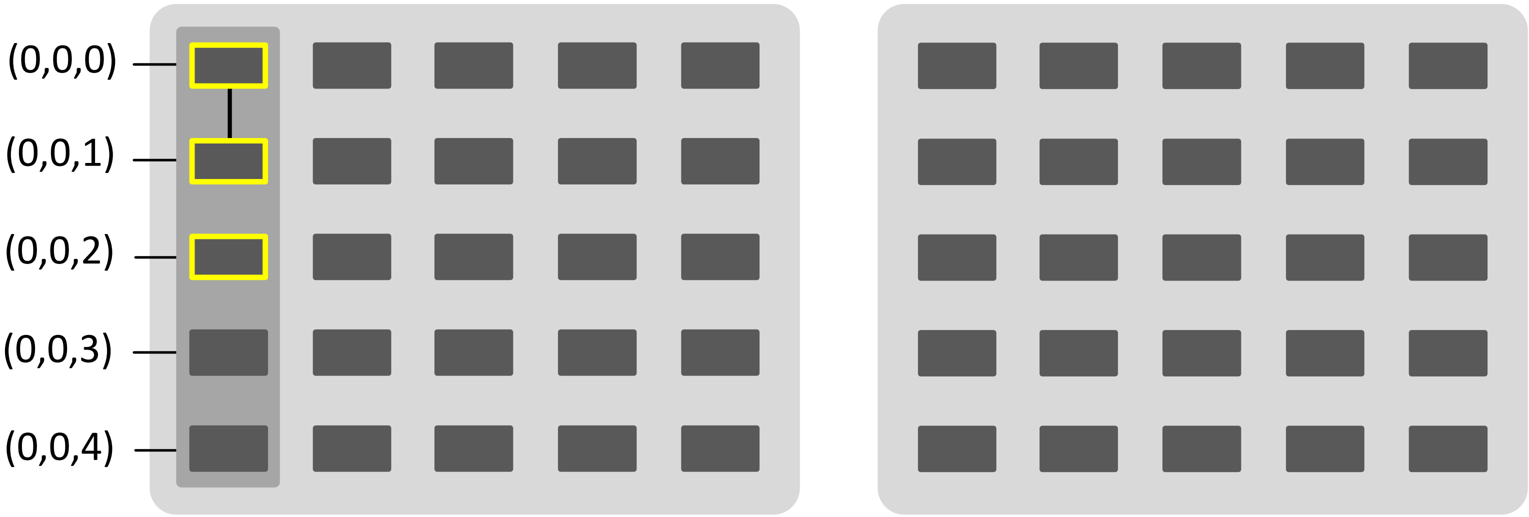

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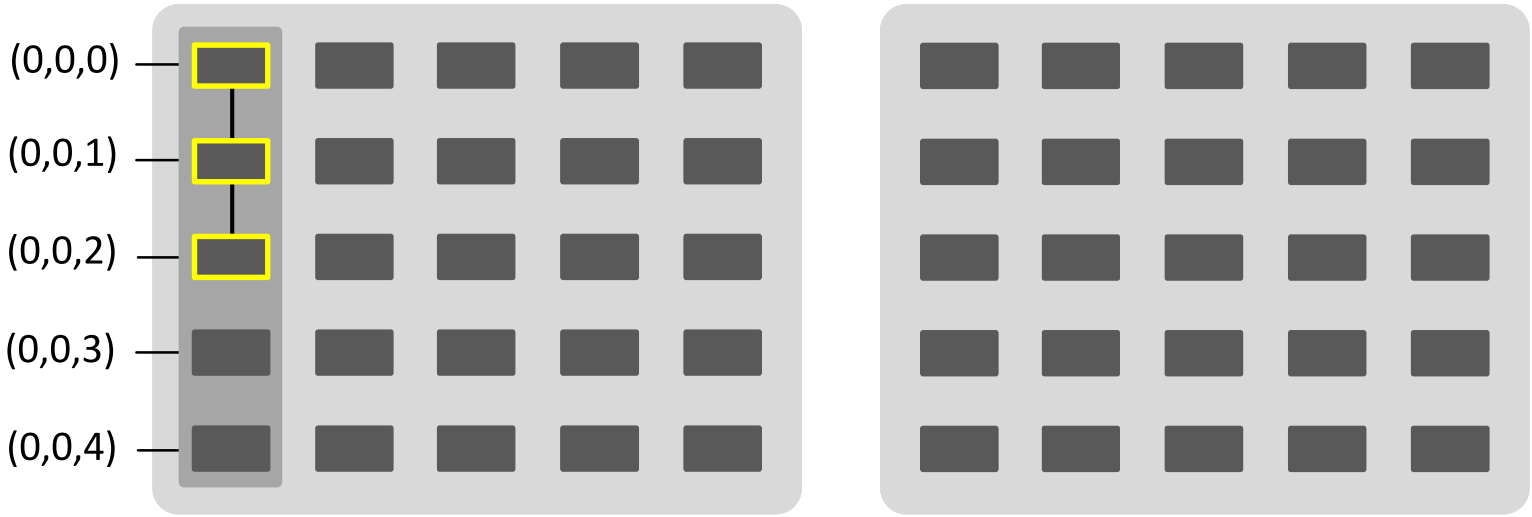

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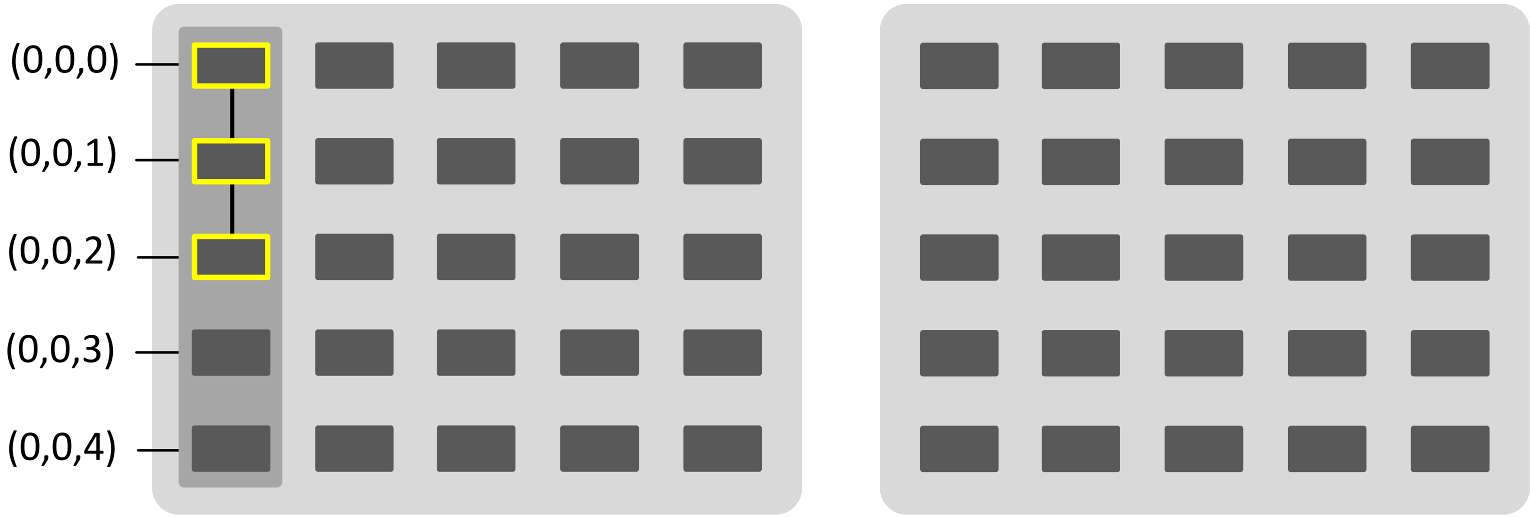

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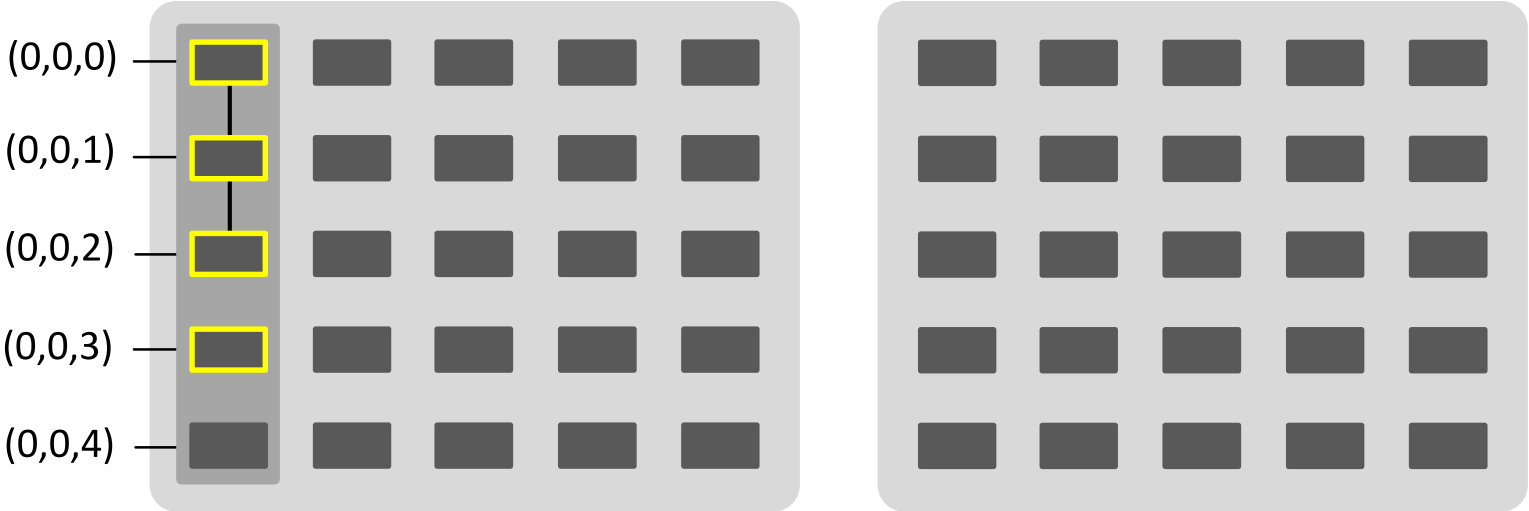

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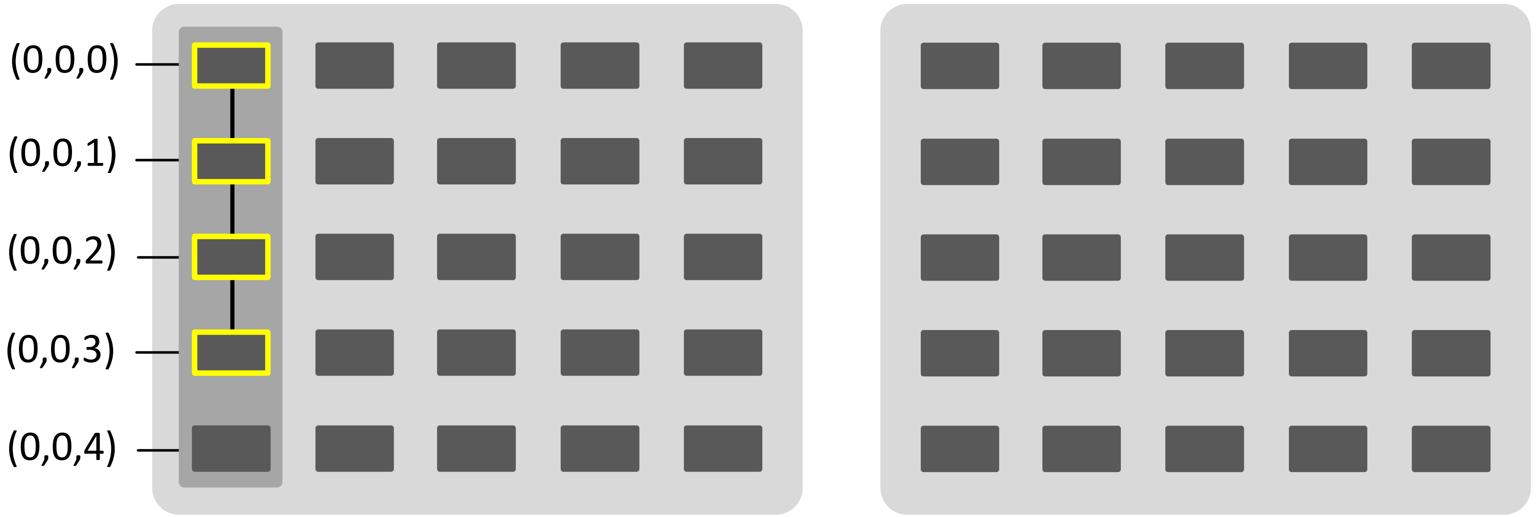

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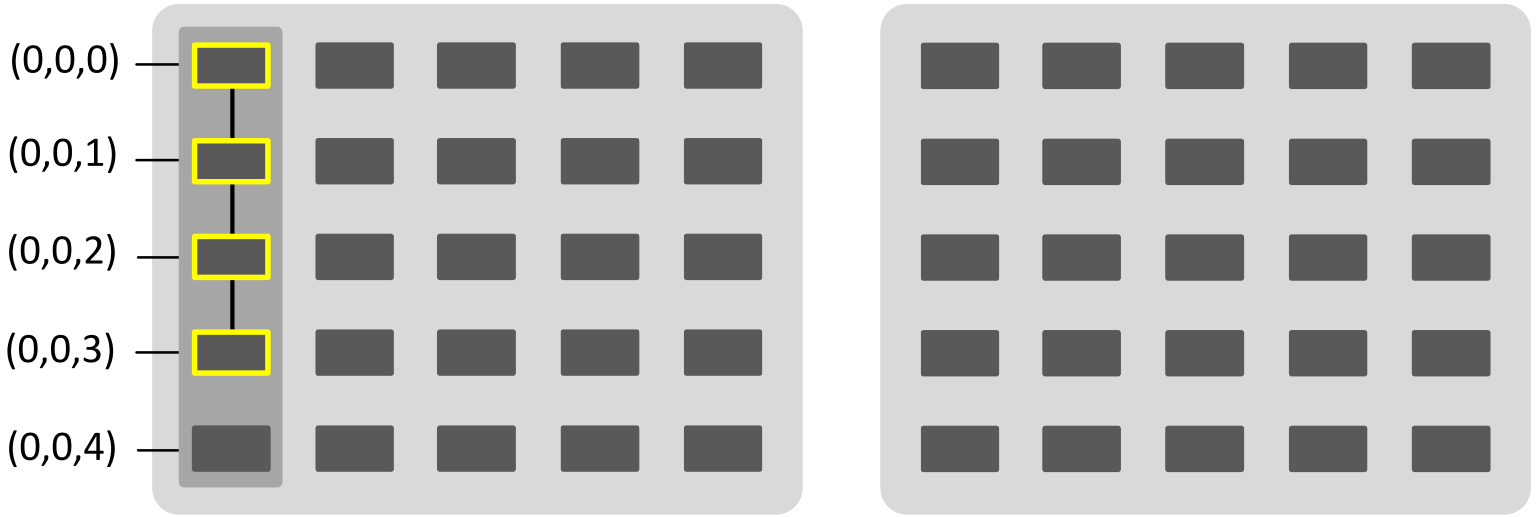
E *Example:* $q = 5$

Take Routers $(0,0,.)$

$$X = \{1, 4\}$$



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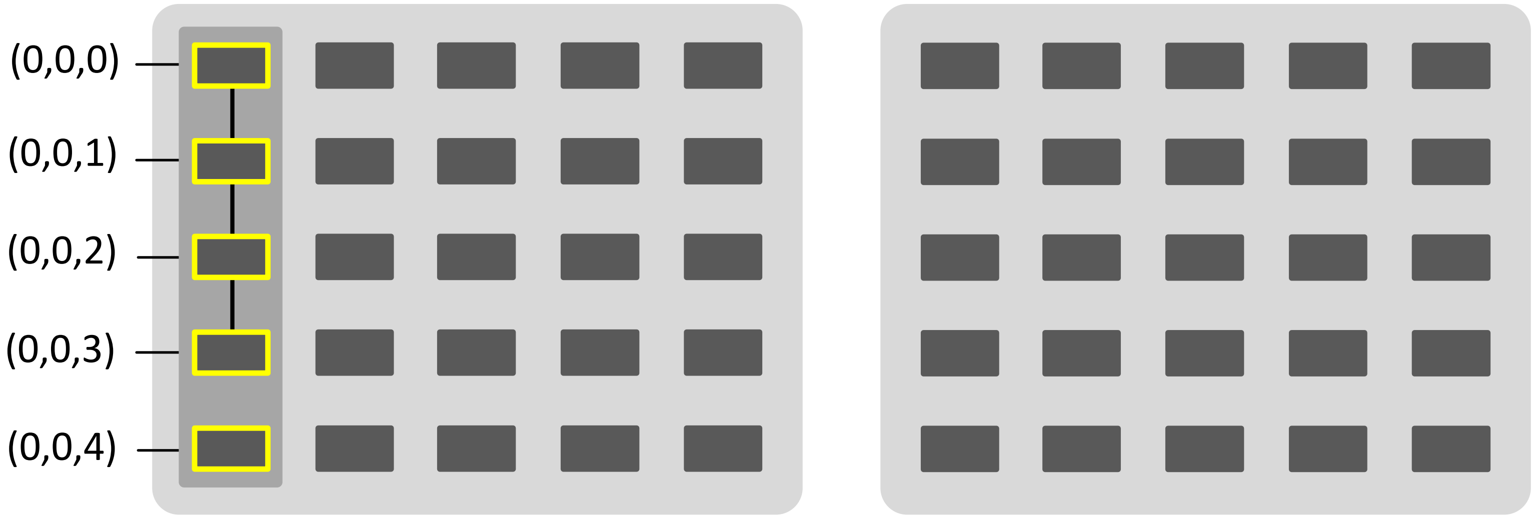

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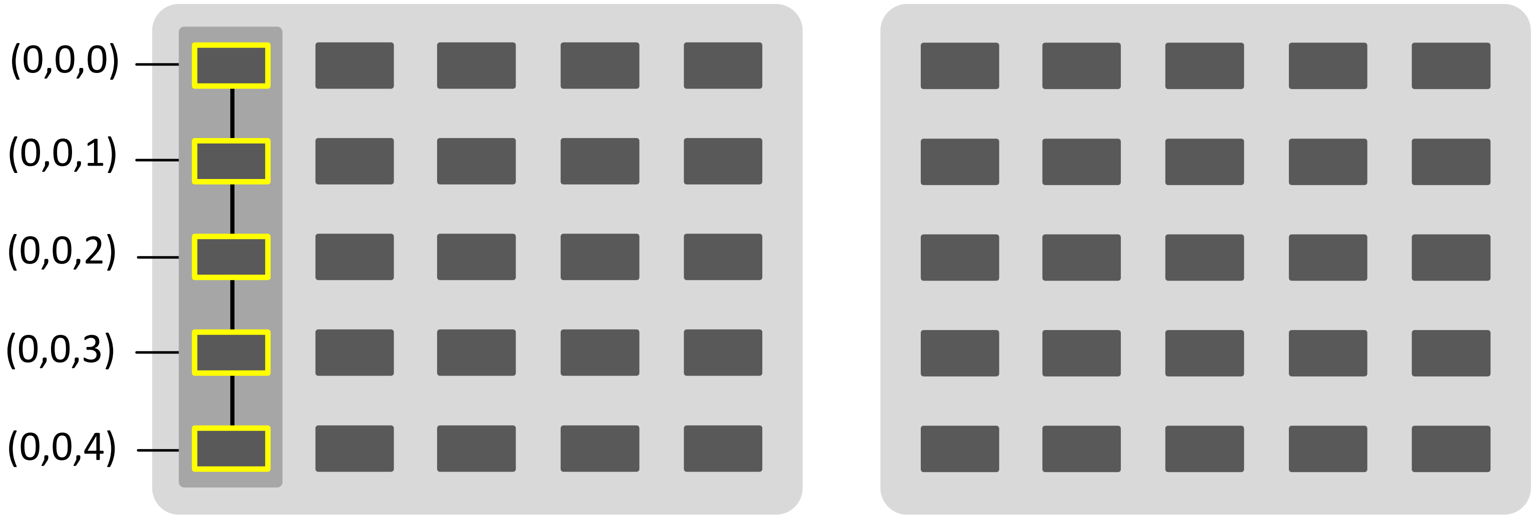

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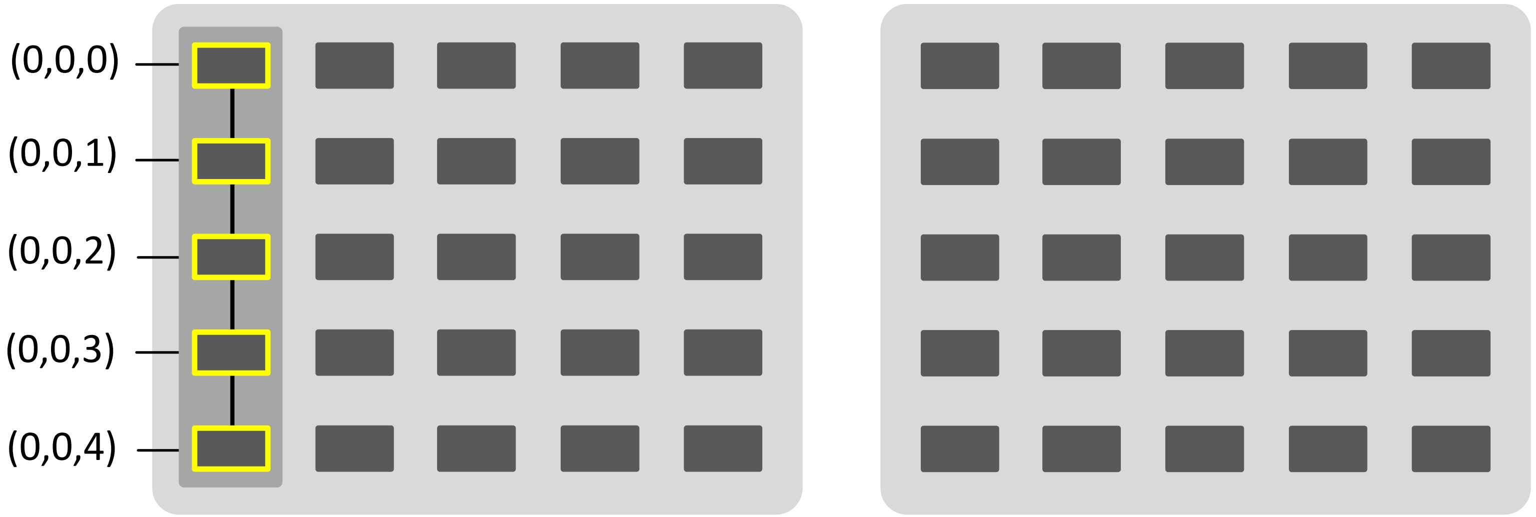

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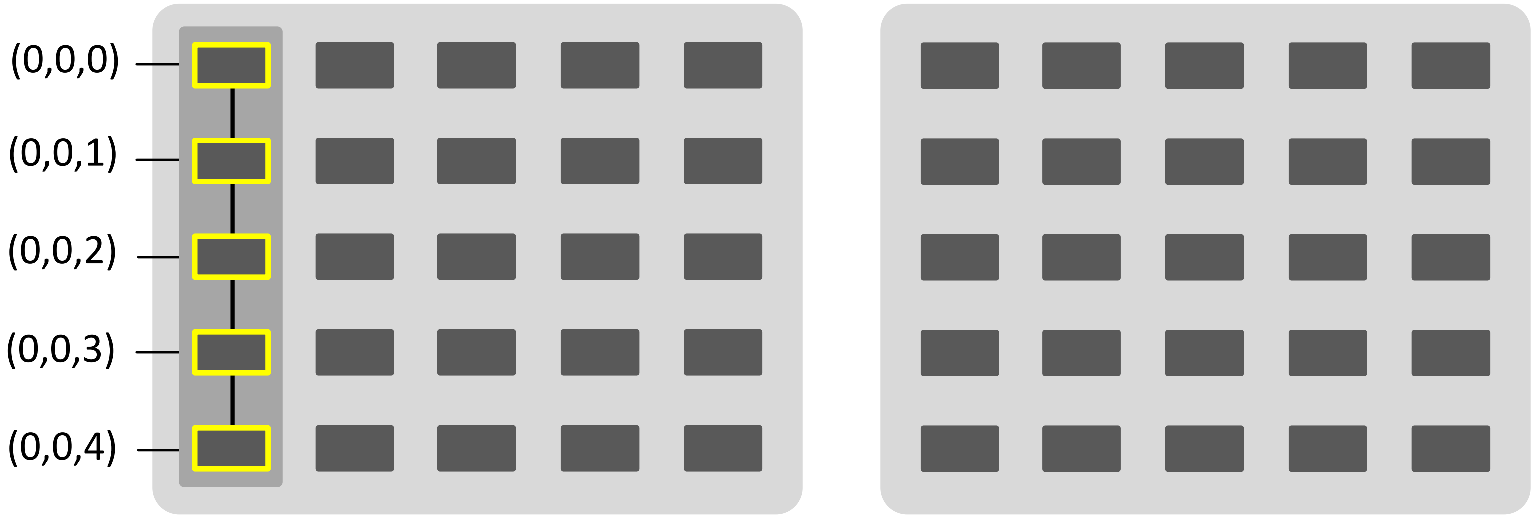

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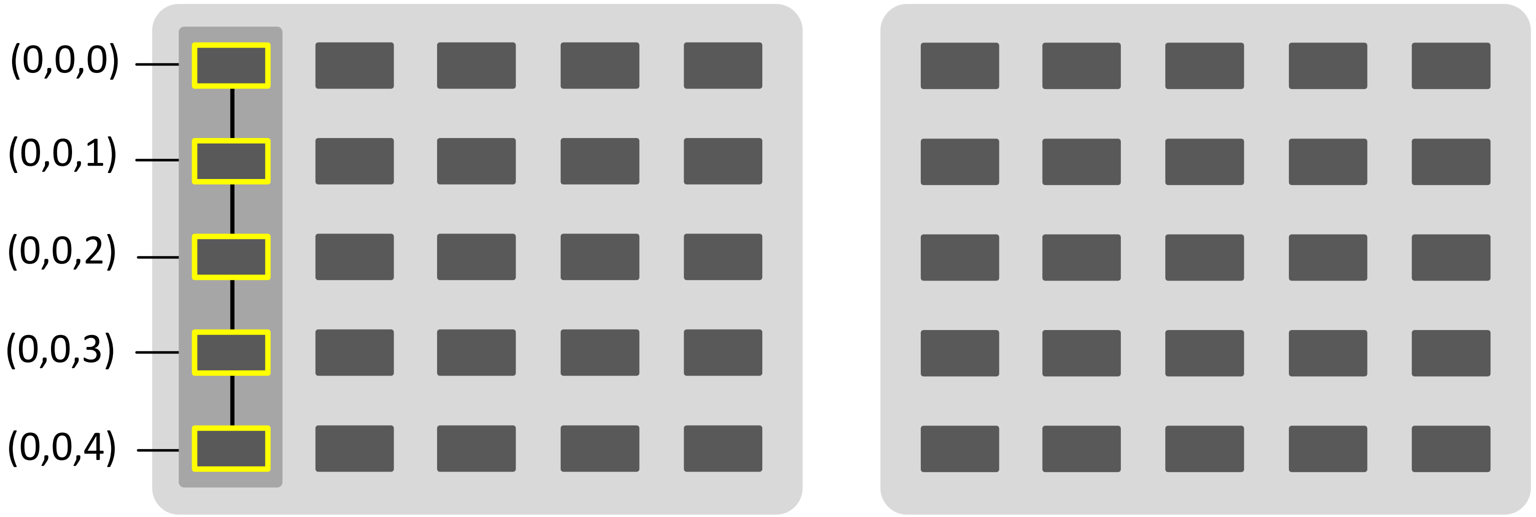

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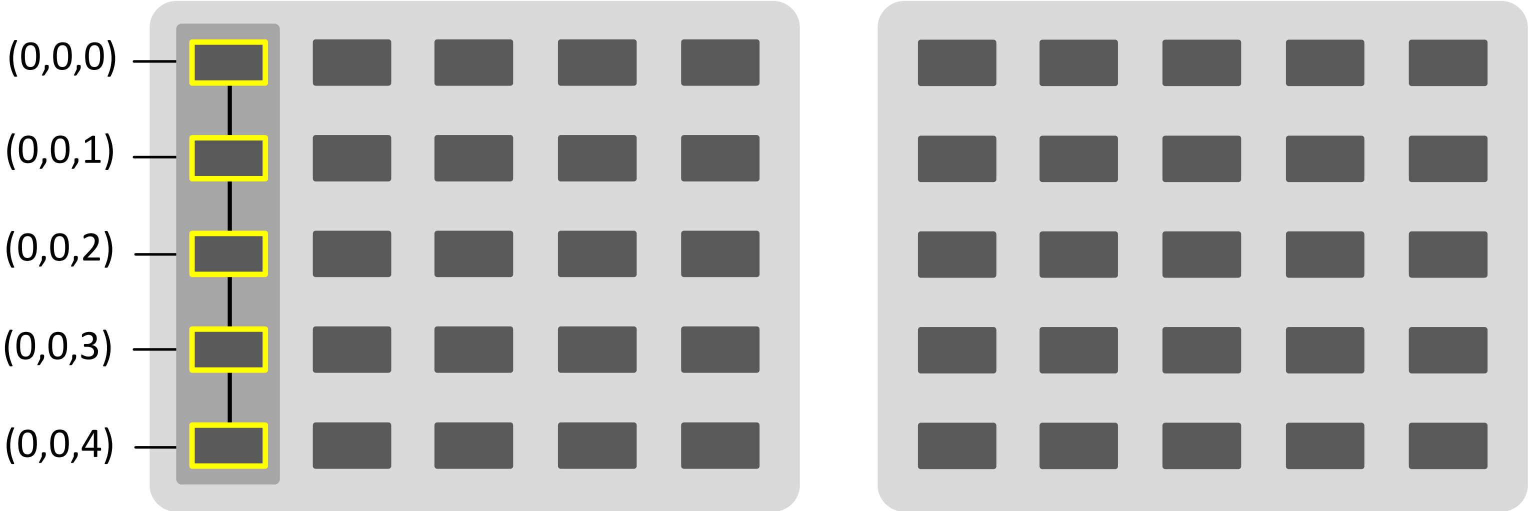

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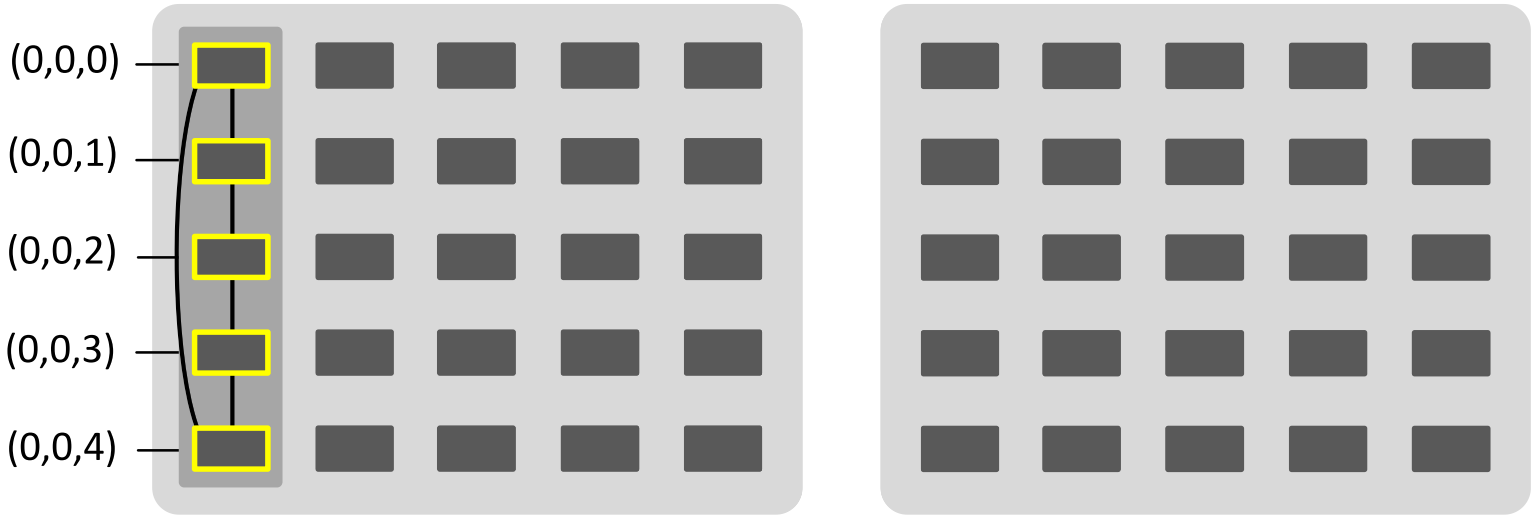

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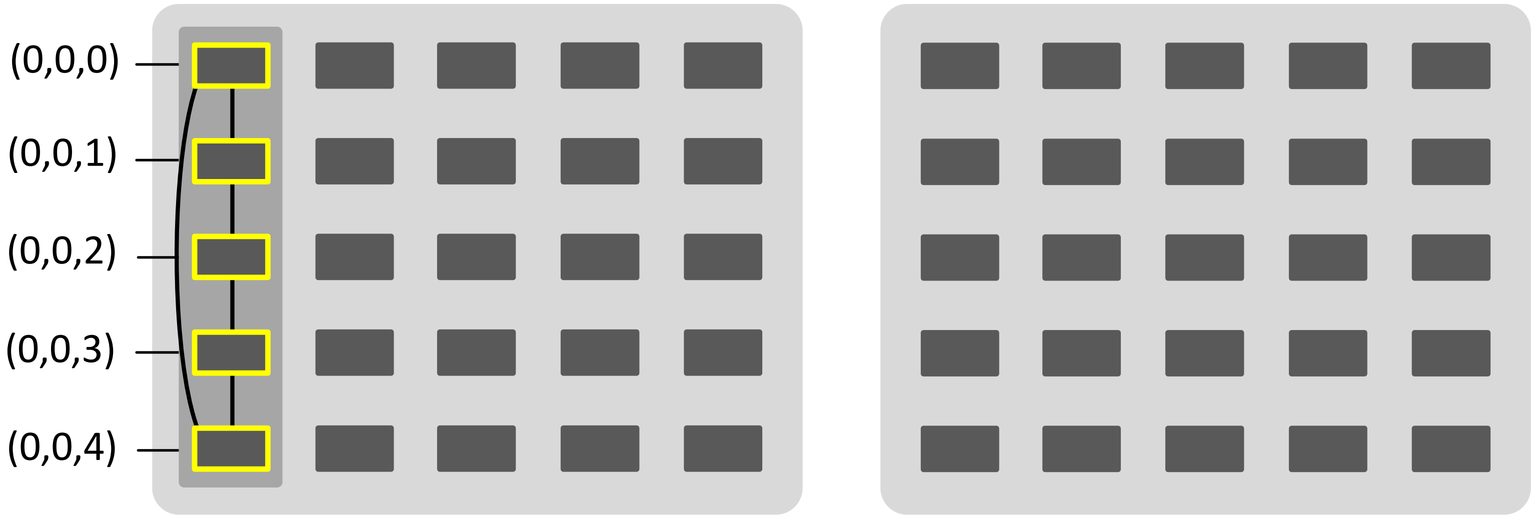

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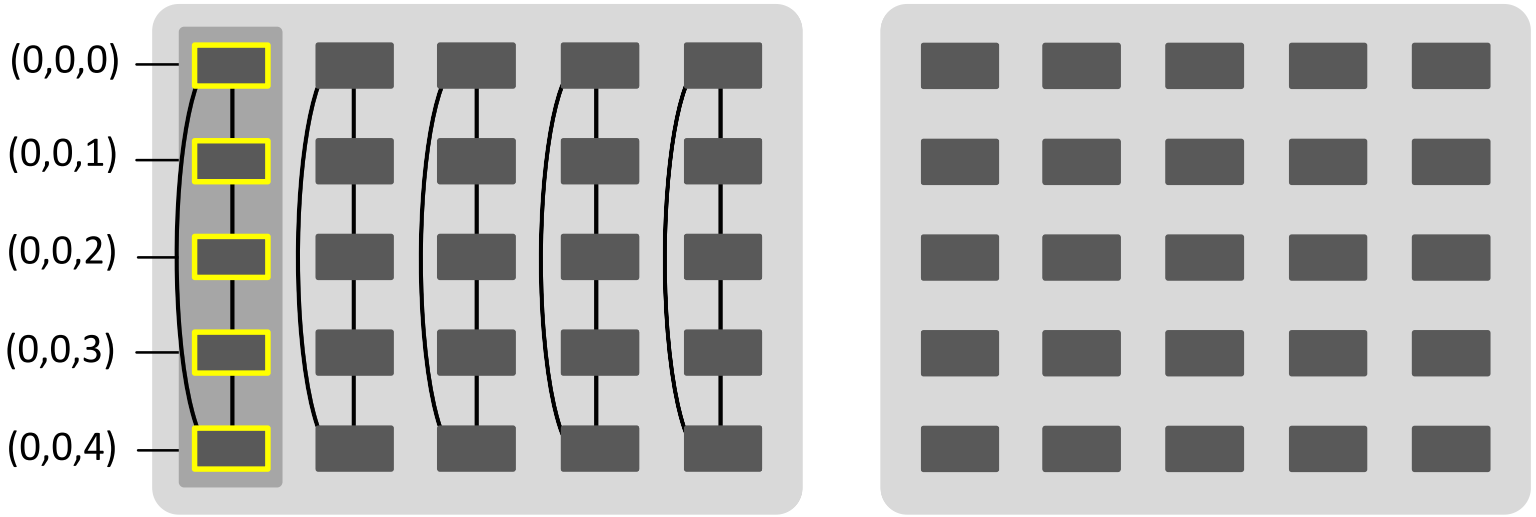

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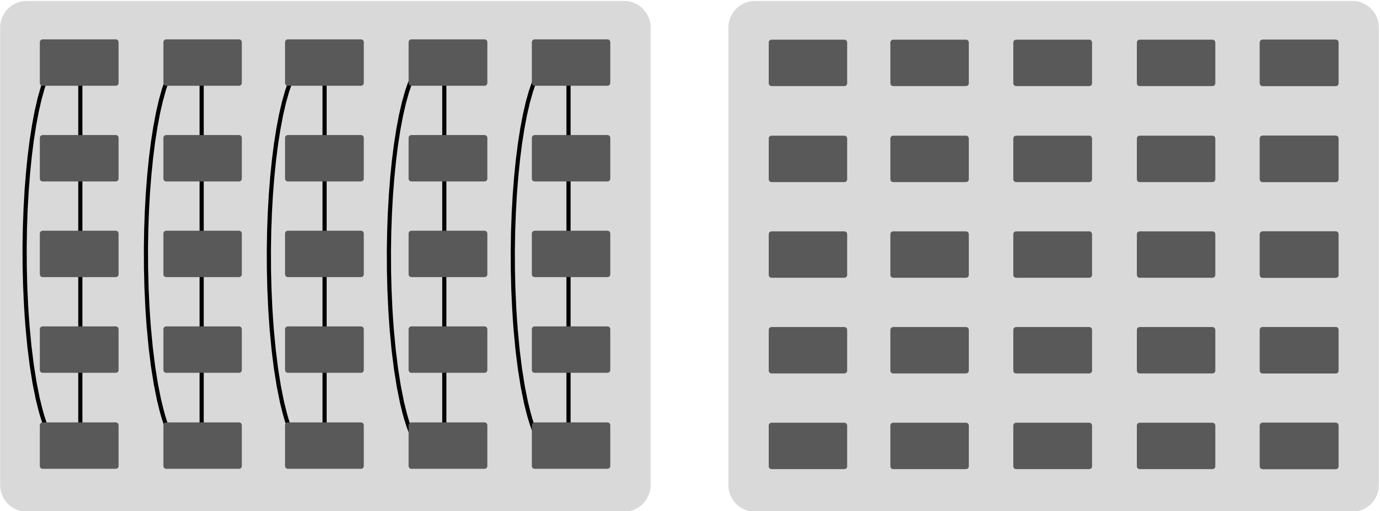

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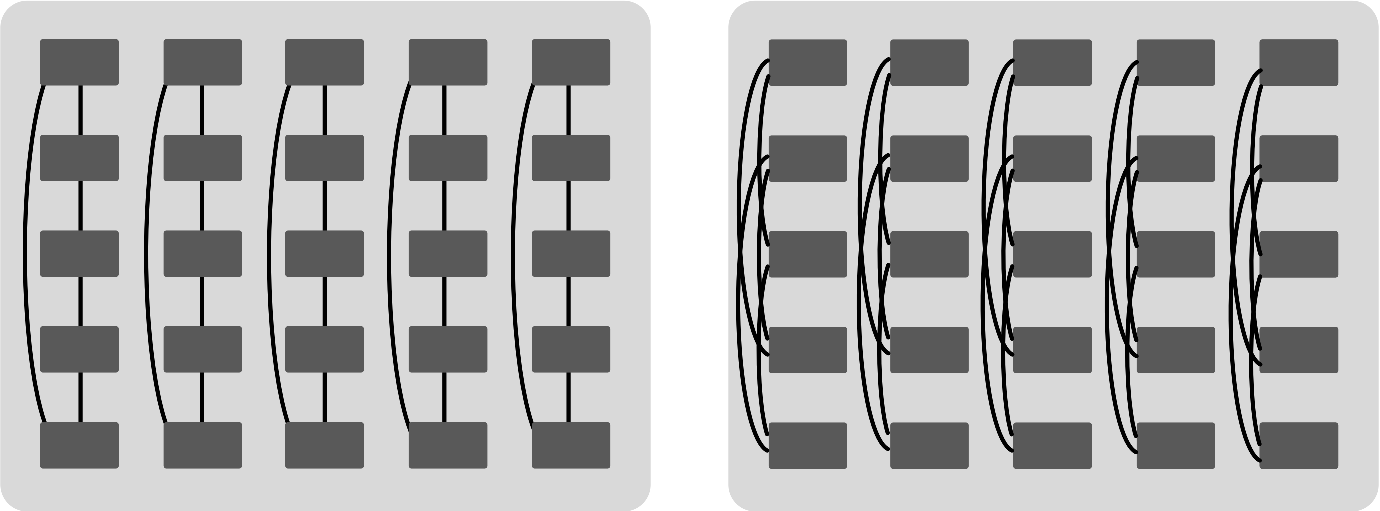

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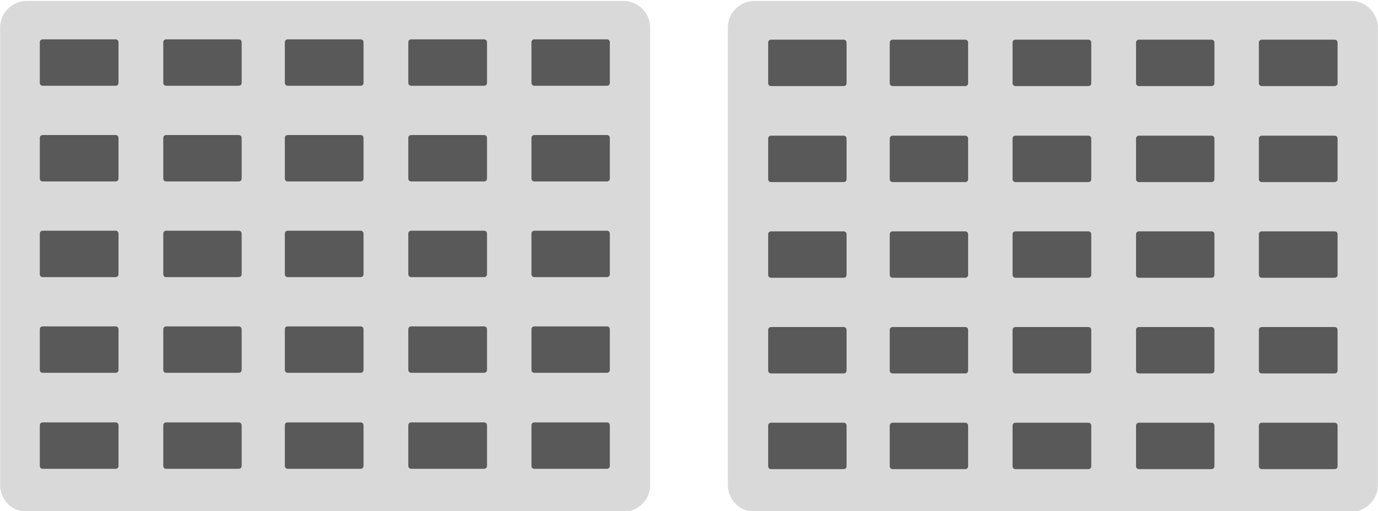

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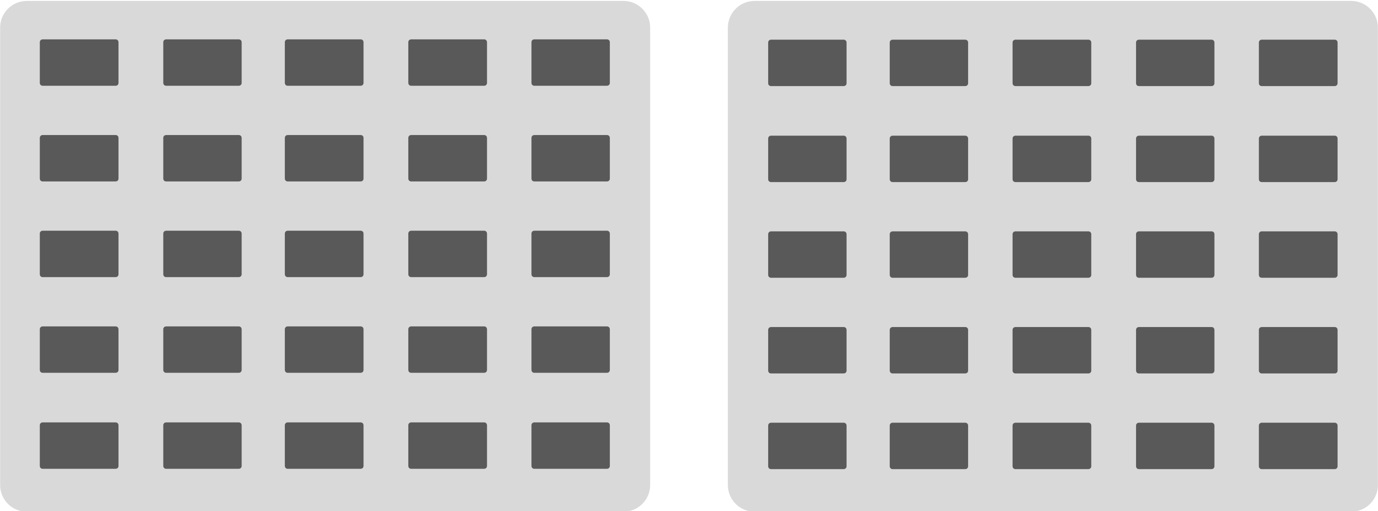
7 *Inter-group connections*



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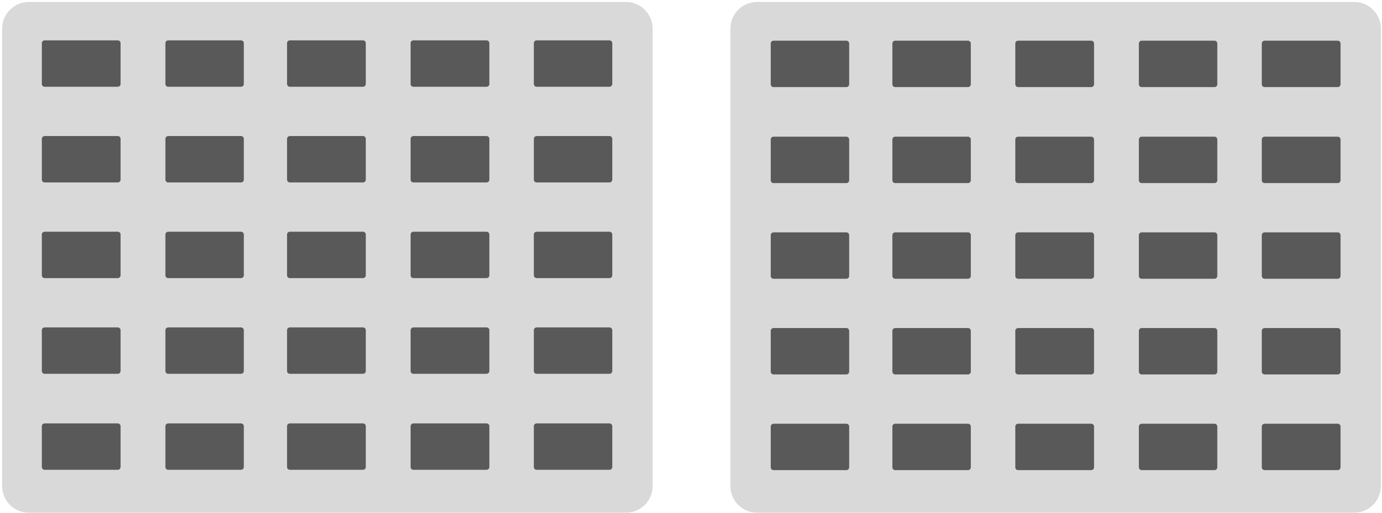
Router $(0, x, y) \leftrightarrow (1, m, c)$



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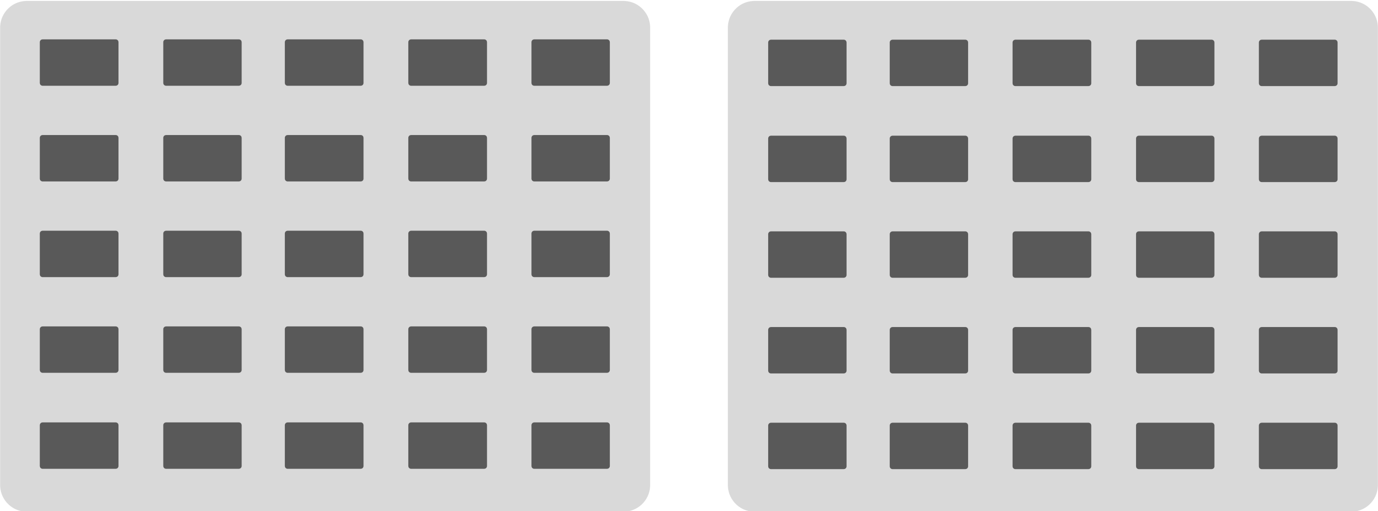

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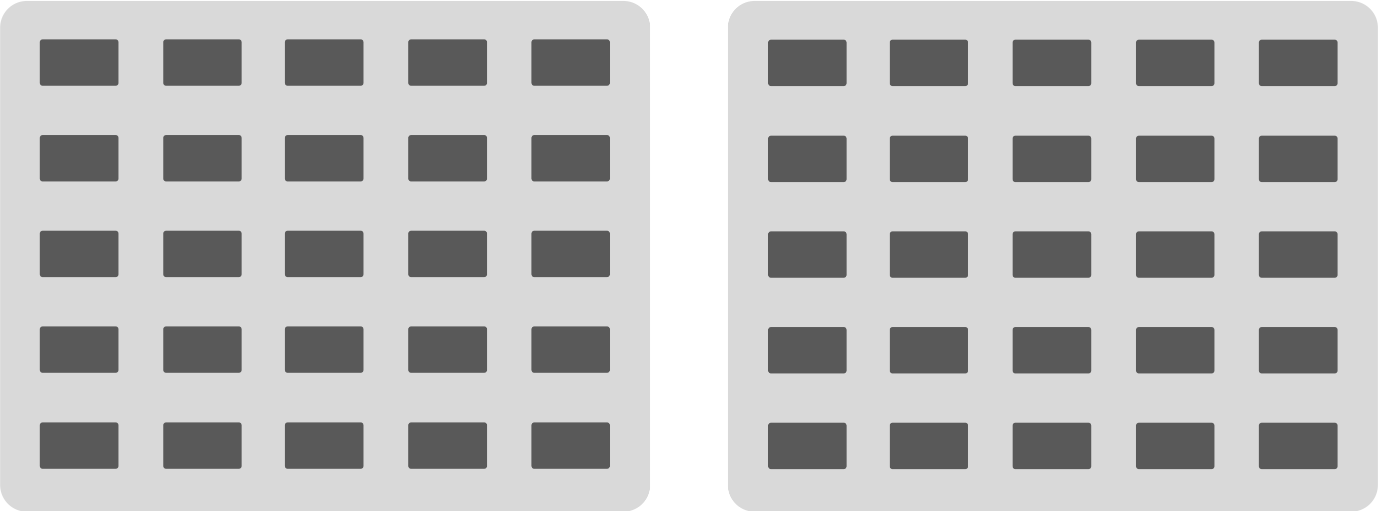

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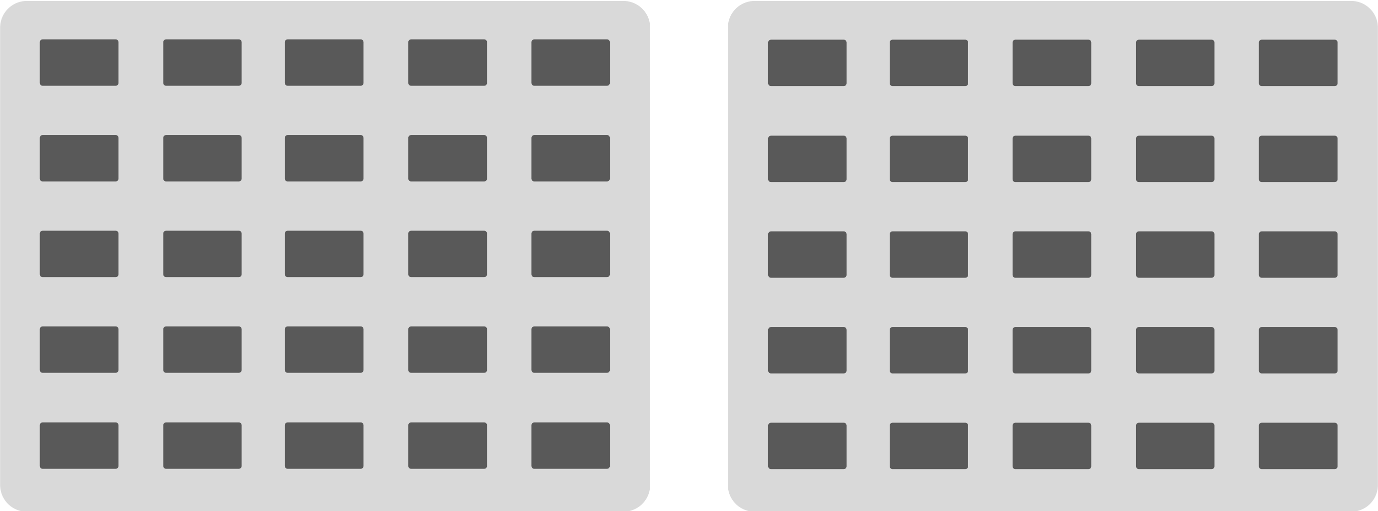

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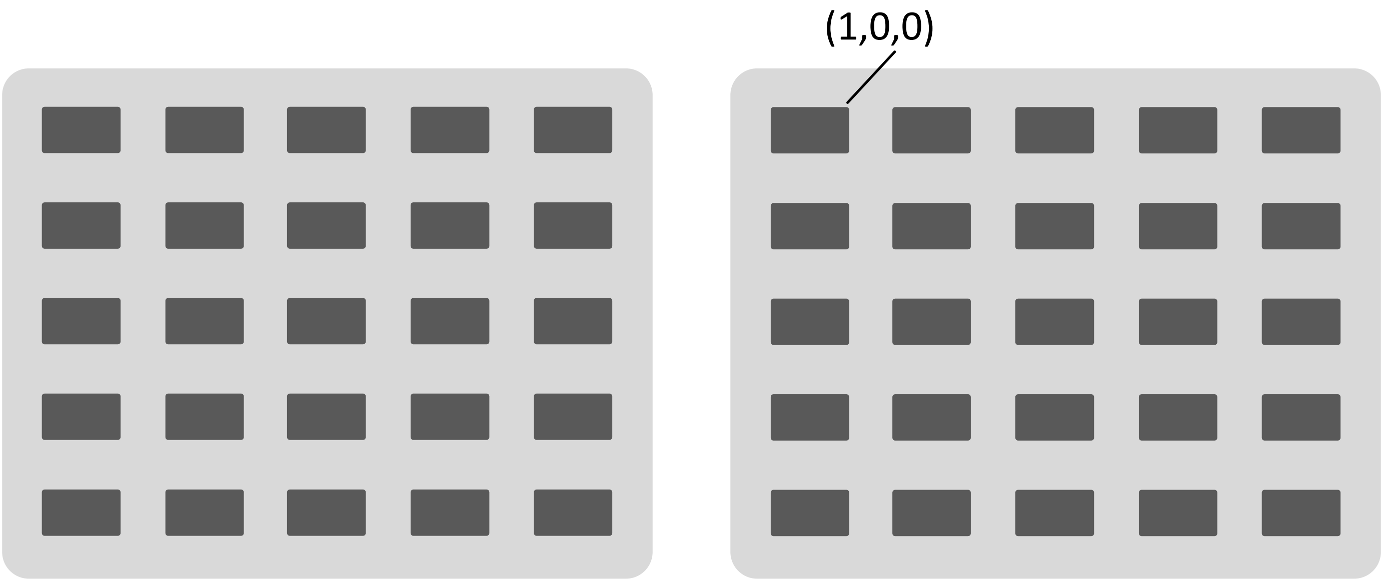

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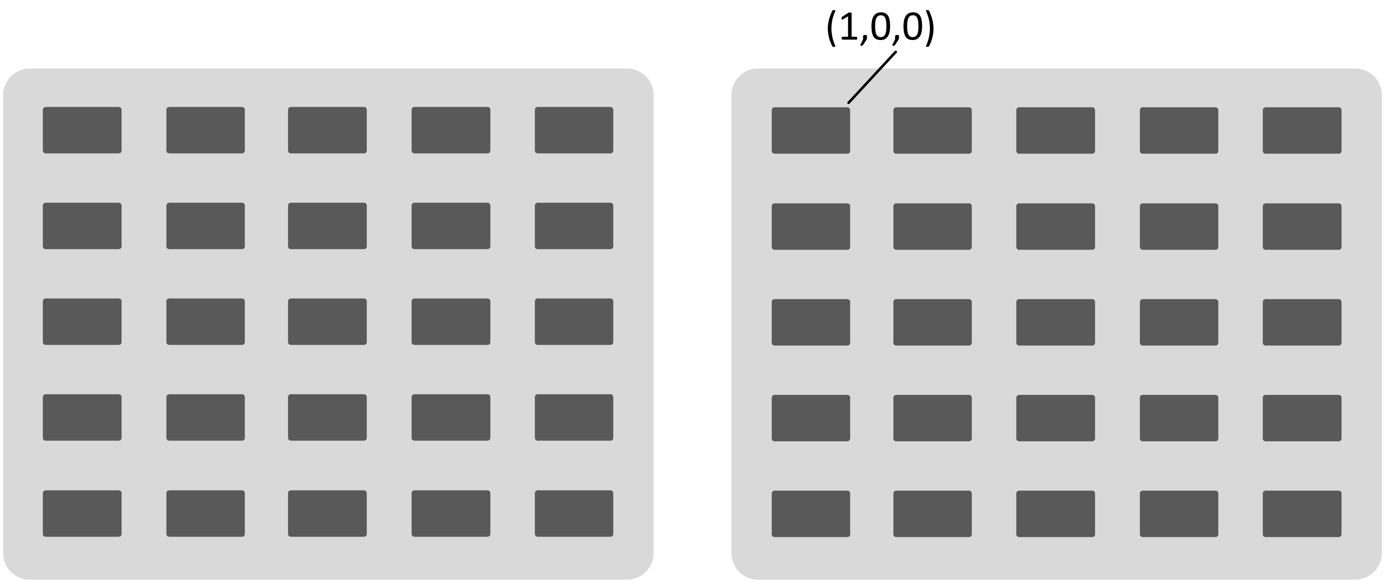

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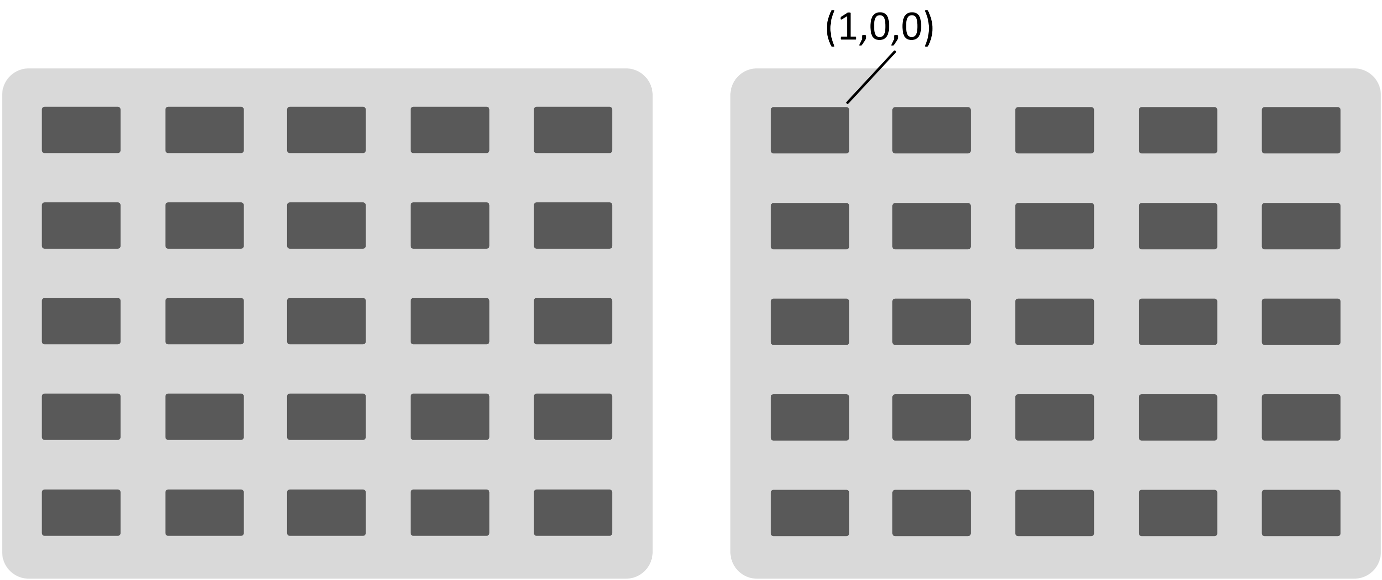

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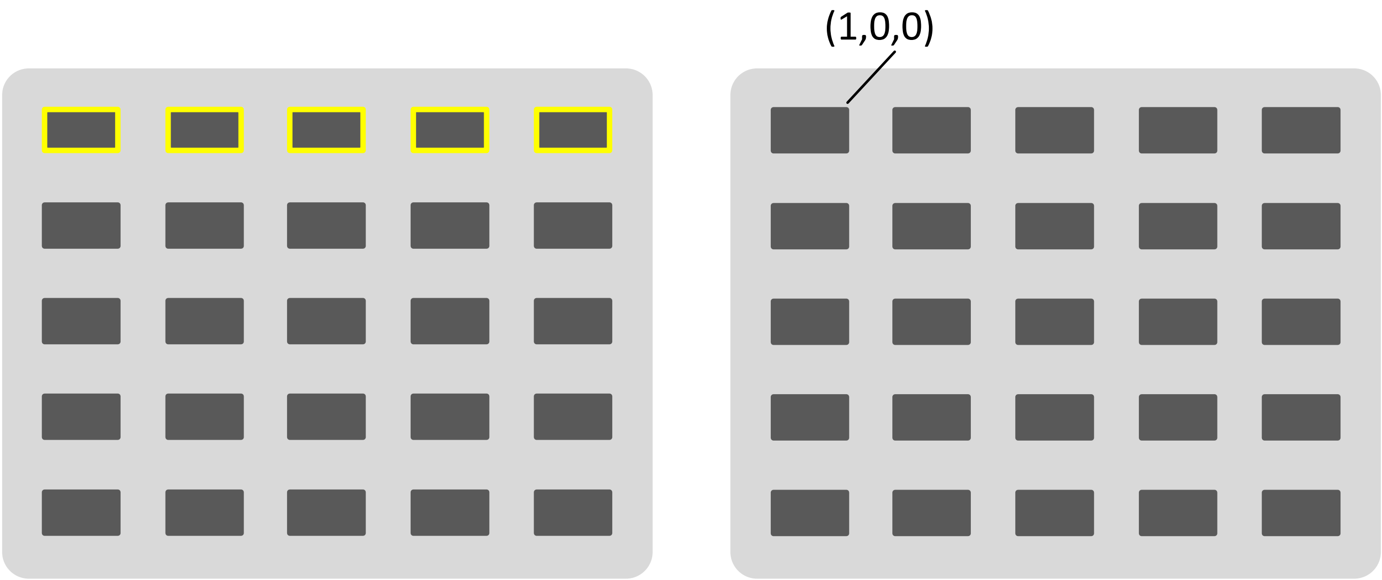

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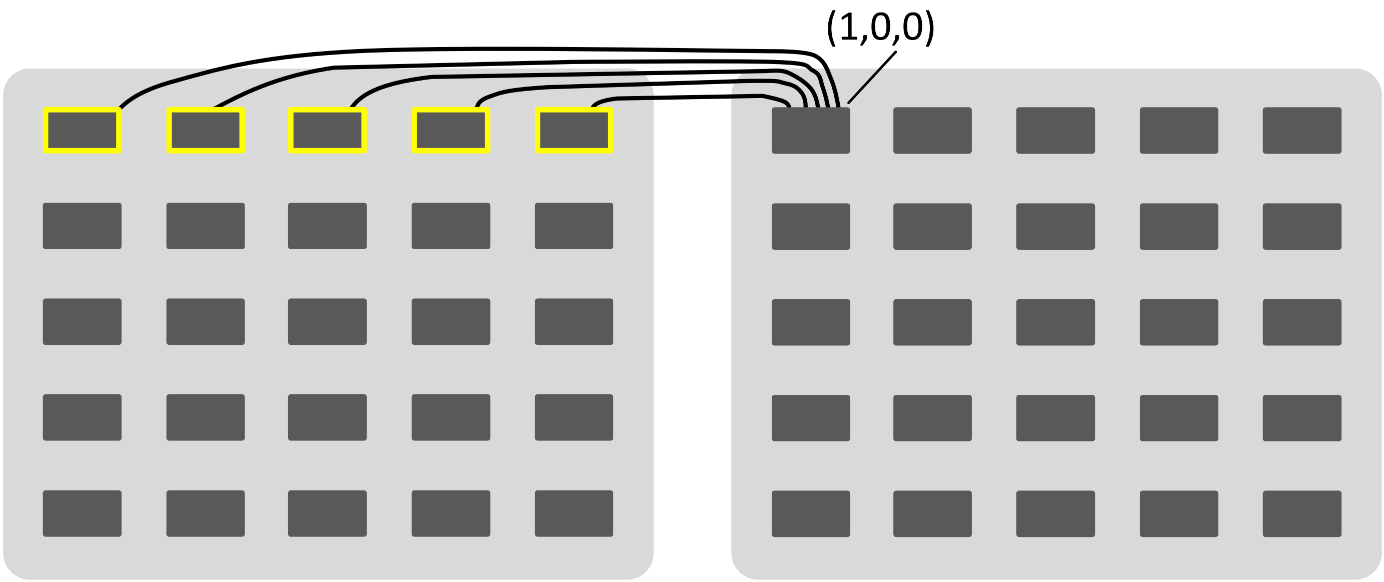

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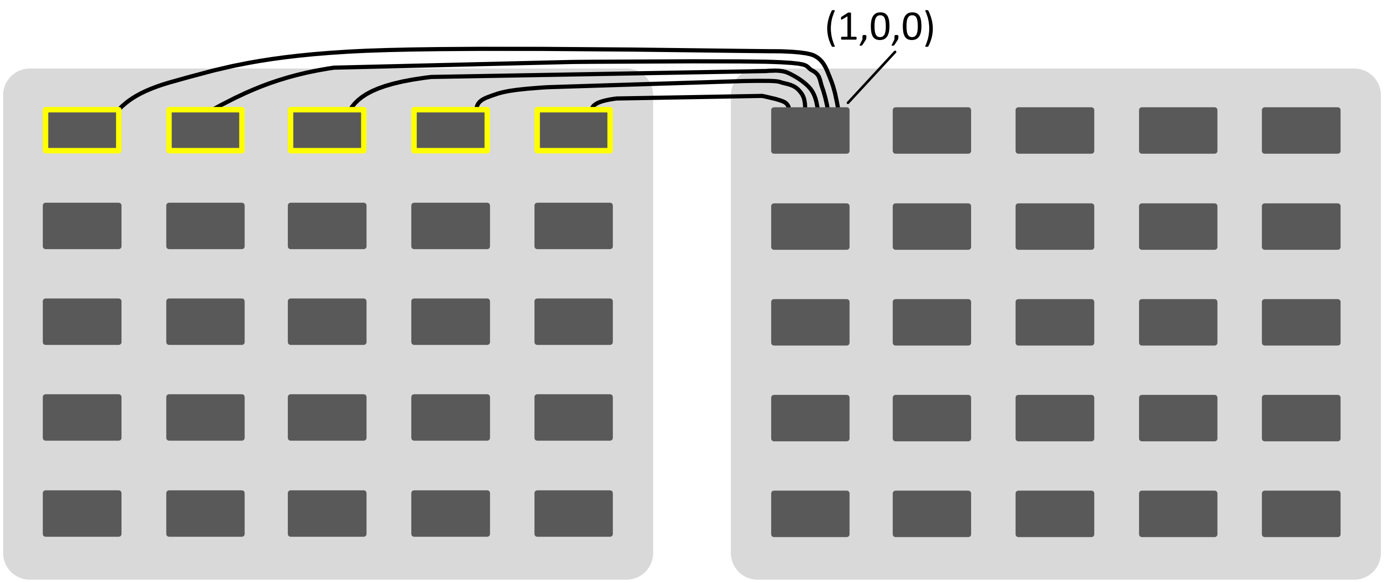

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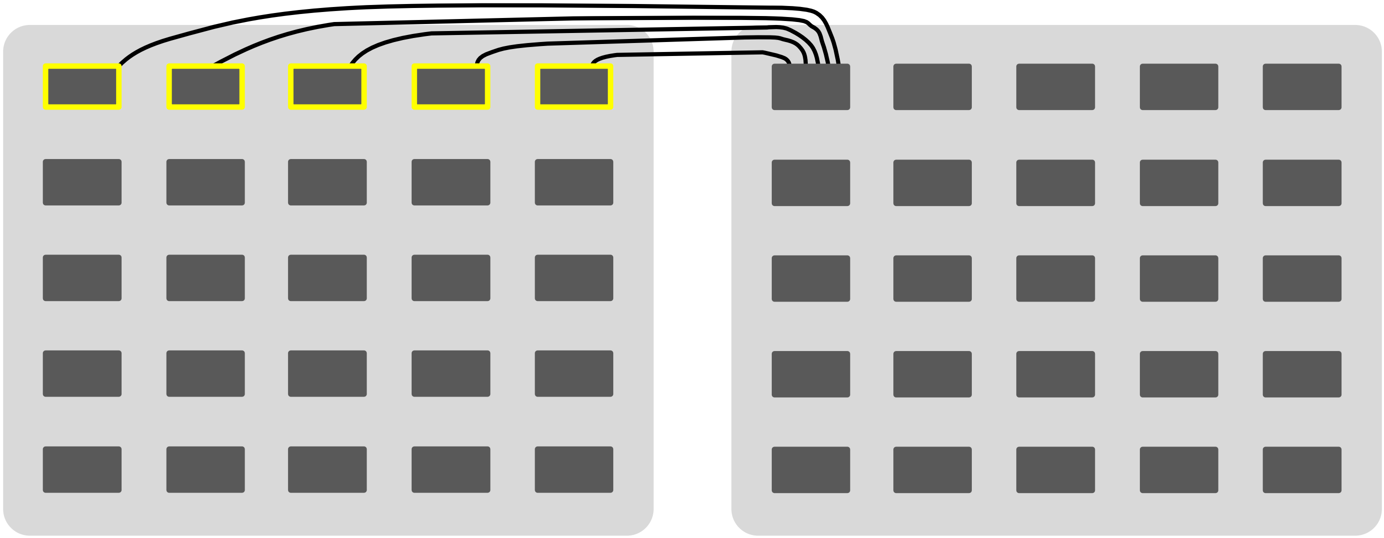

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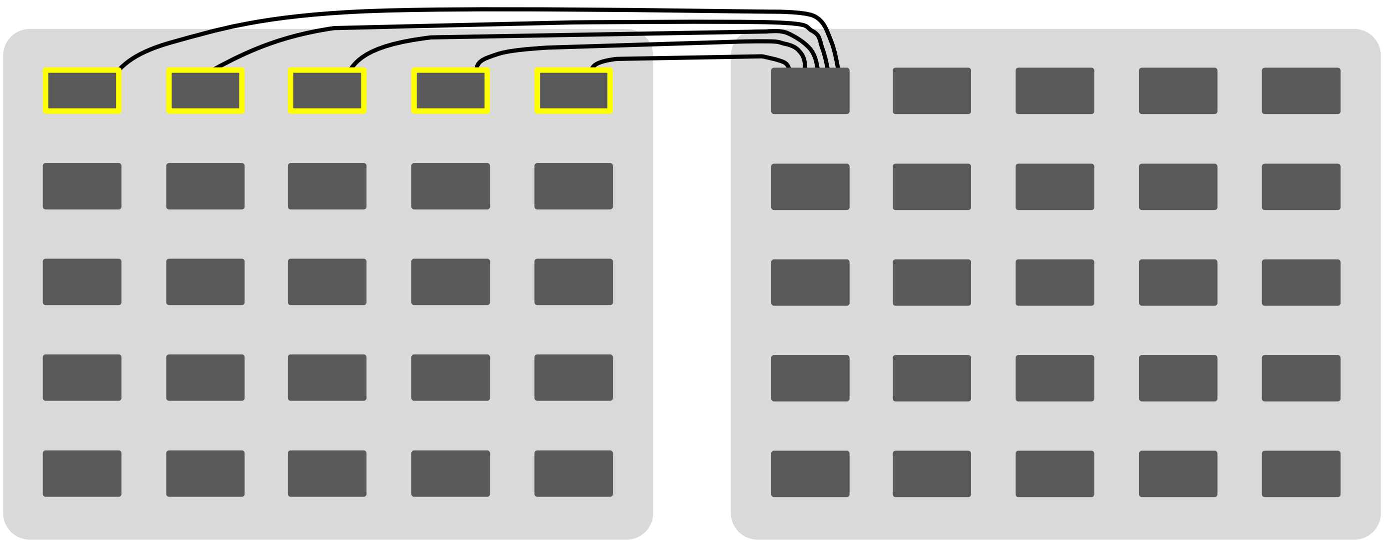

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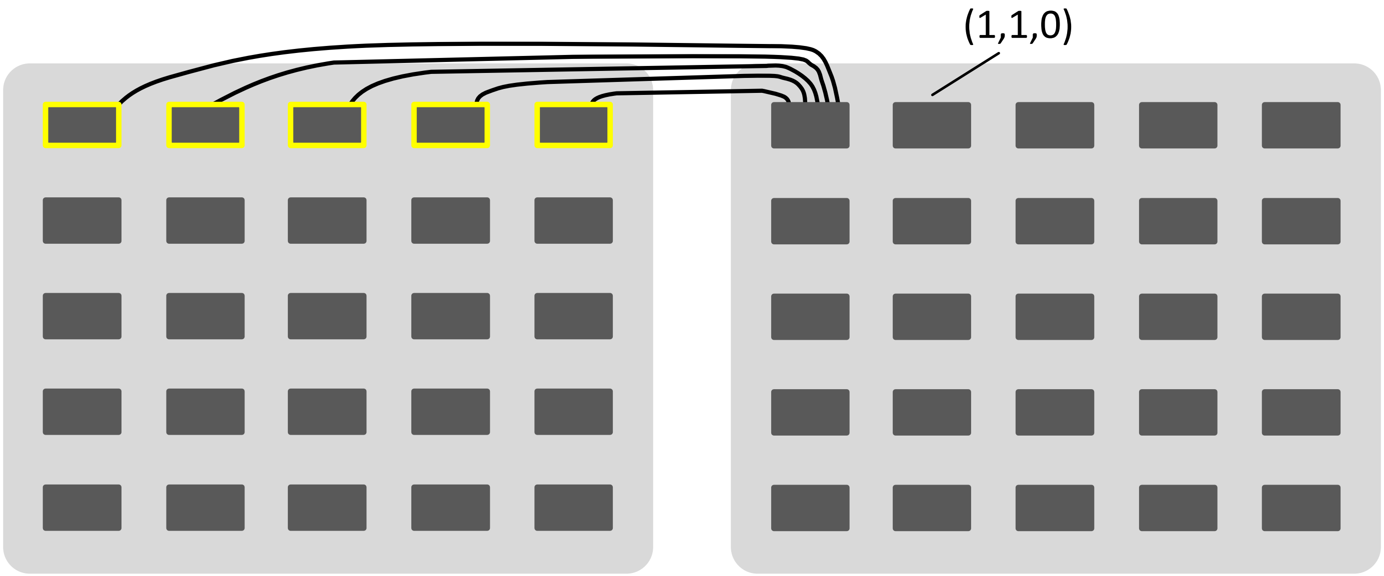

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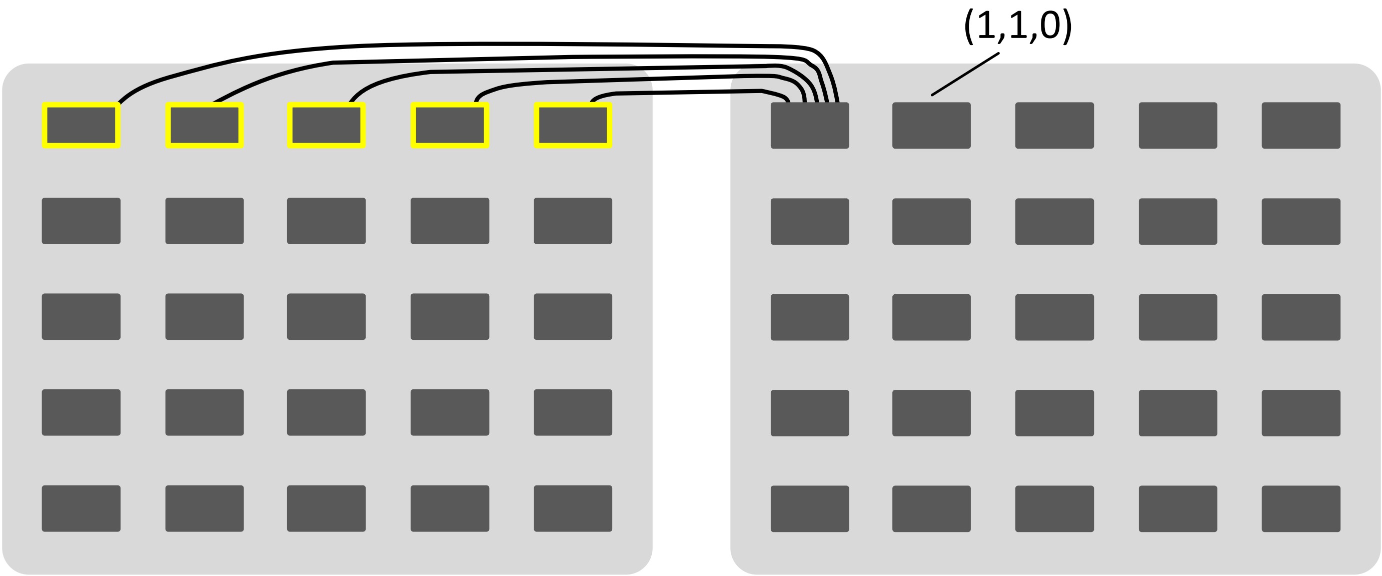

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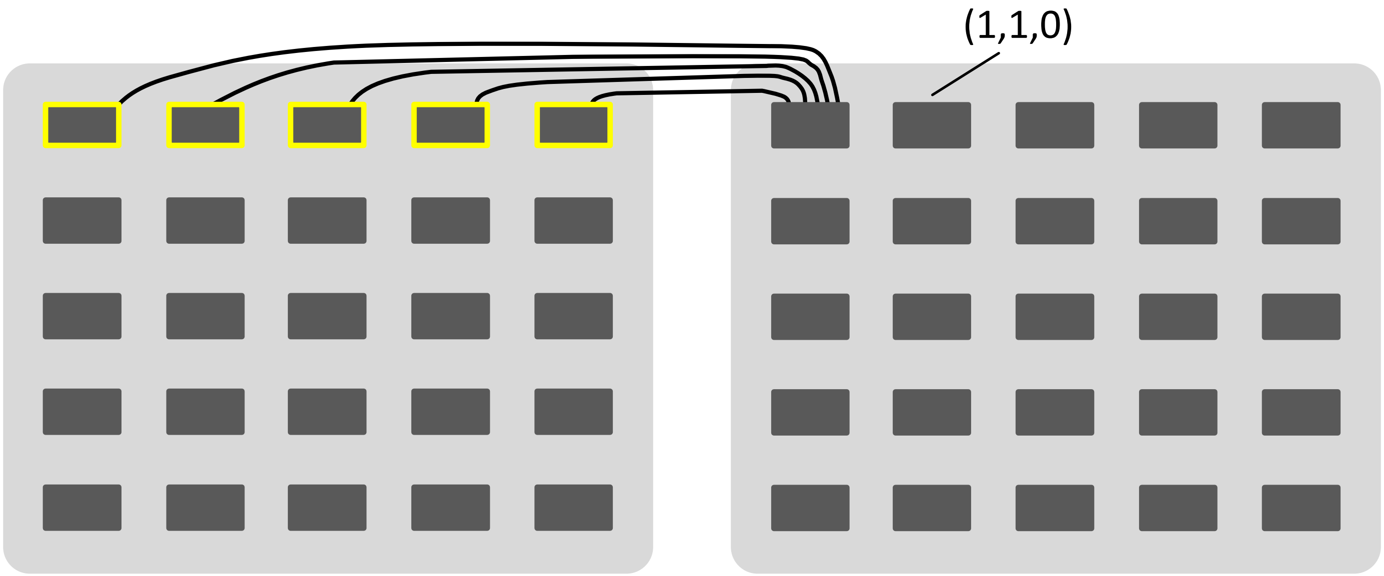

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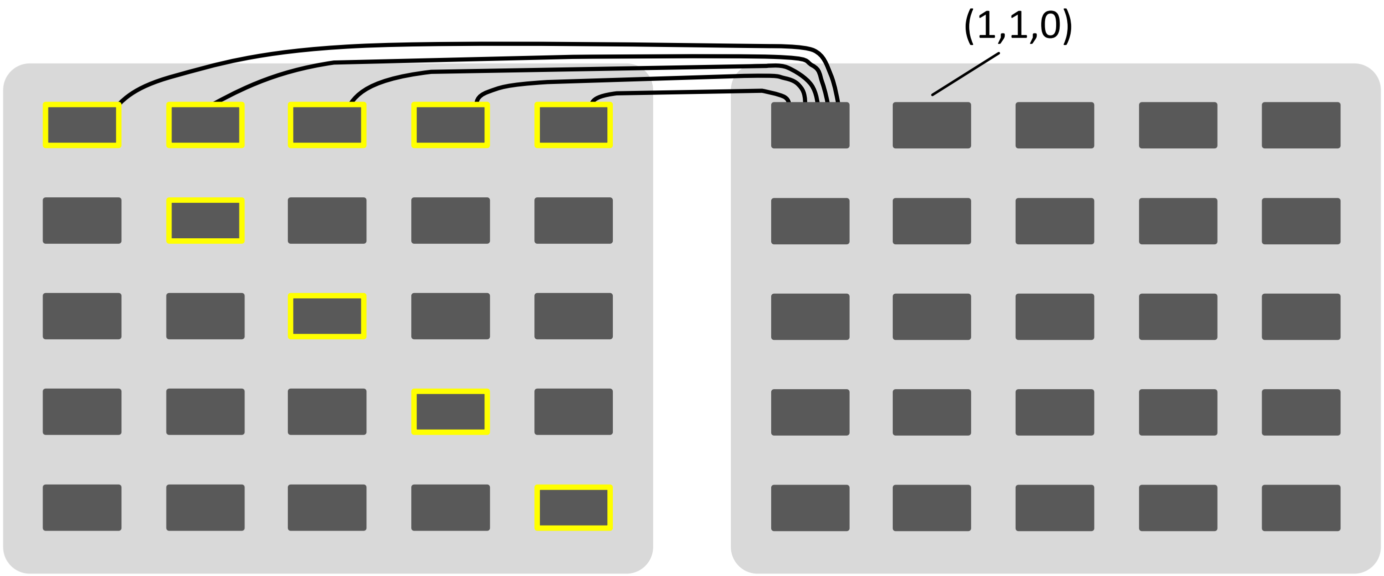

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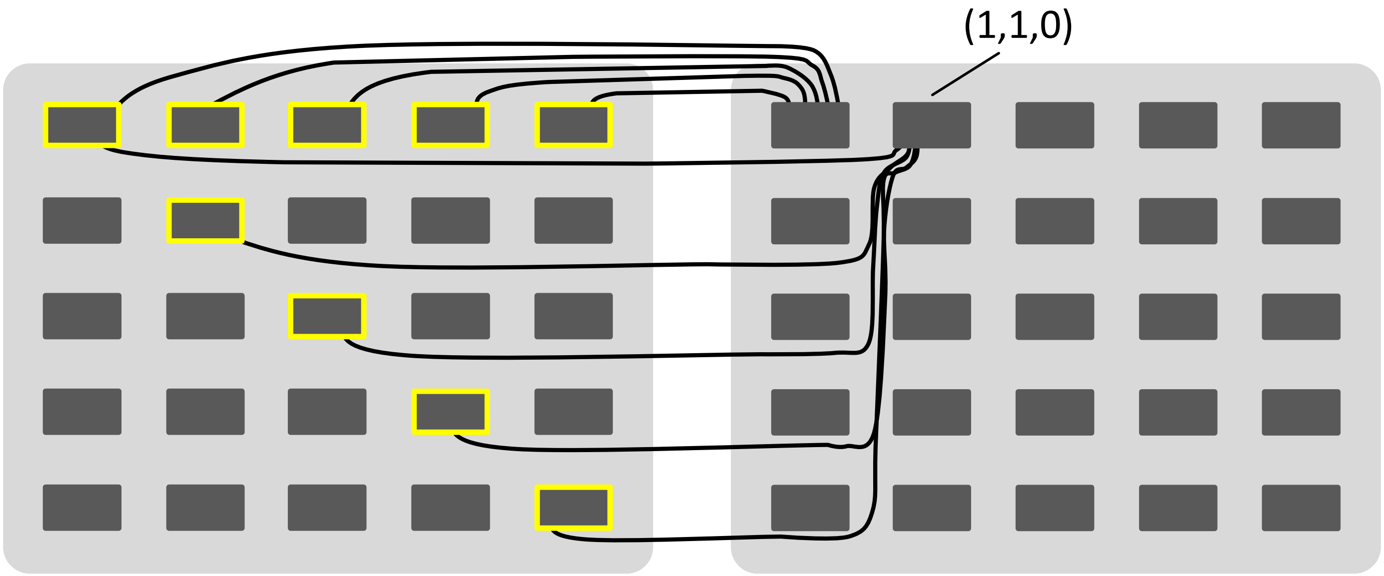

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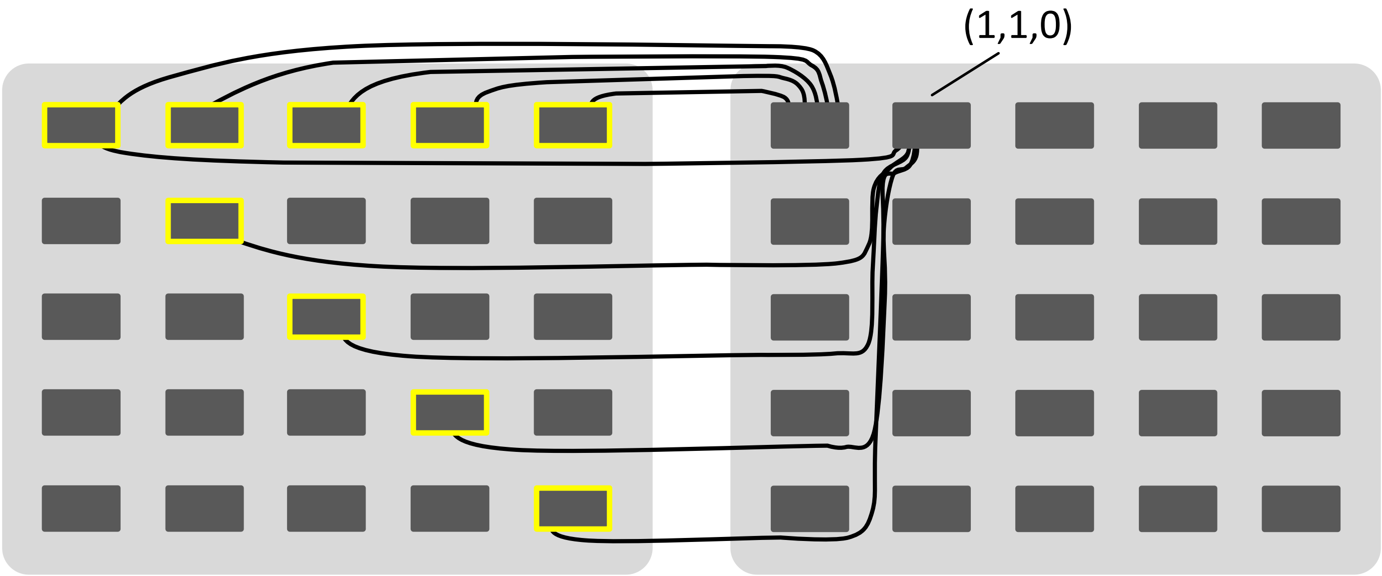

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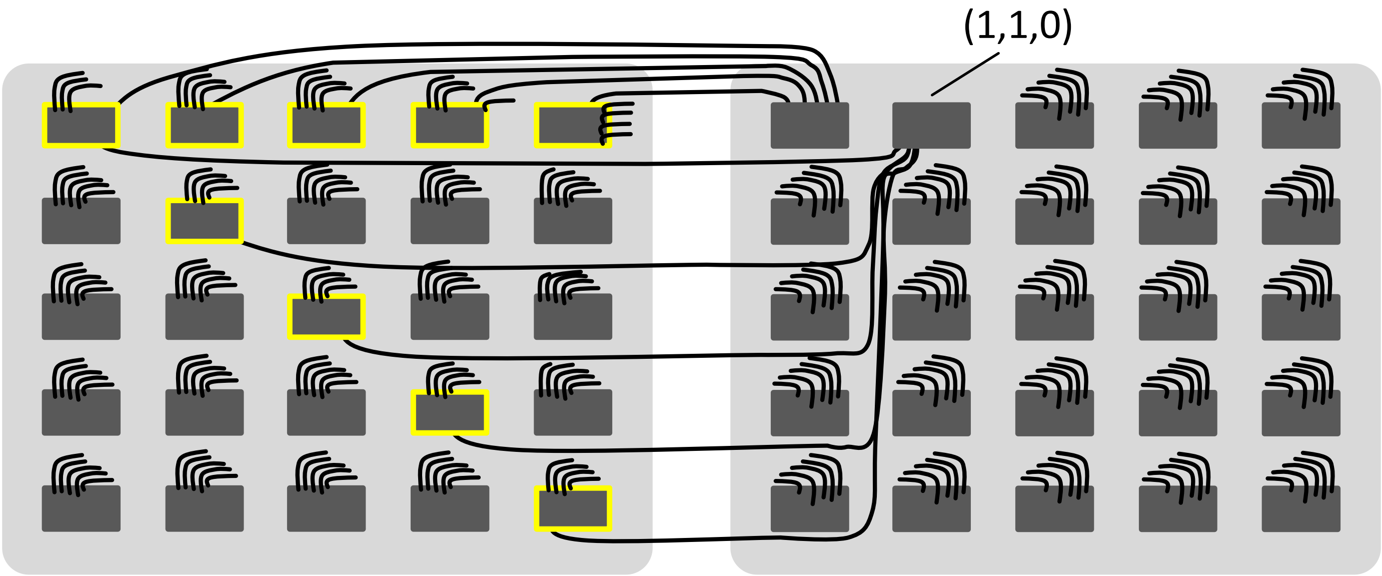
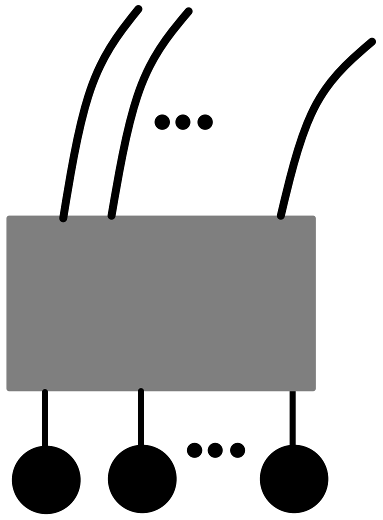


Designing An Efficient Network Topology

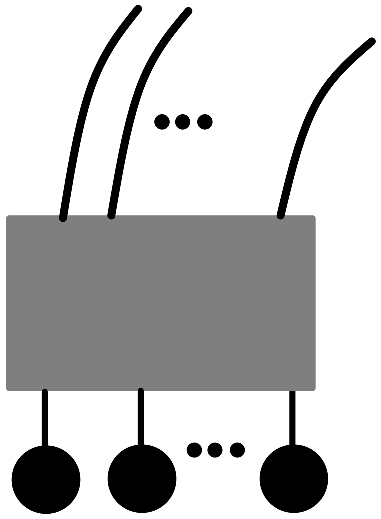
Attaching endpoints: Diameter 2



Designing An Efficient Network Topology

Attaching endpoints: Diameter 2

1 Get load l per router-router channel (average number of routes per channel)

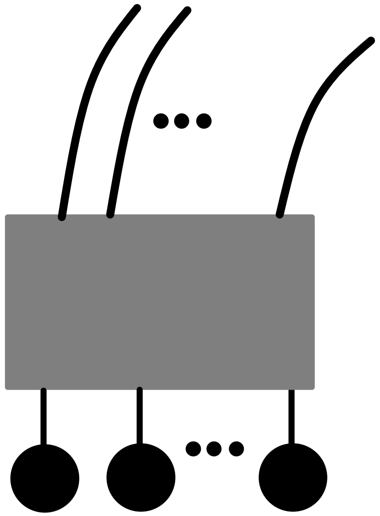


Designing An Efficient Network Topology

Attaching endpoints: Diameter 2

1 Get load *l* per router-router channel (average number of routes per channel)

$$l = \frac{total\ number\ of\ routes}{total\ number\ of\ channels}$$



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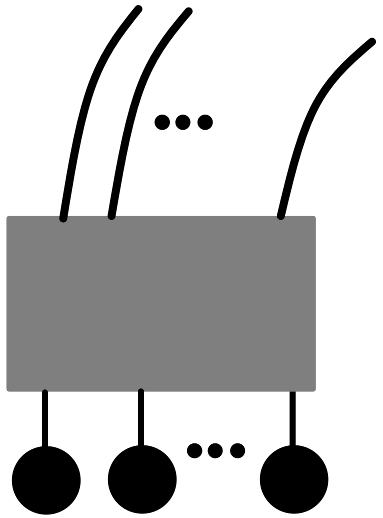

Designing An Efficient Network Topology

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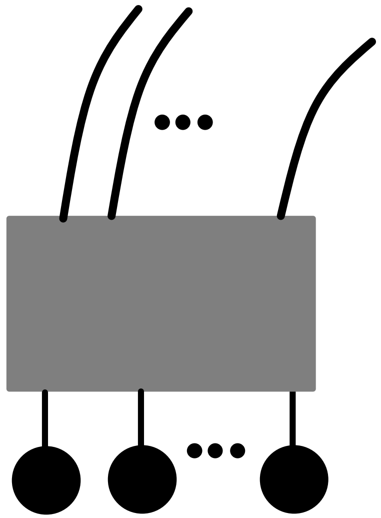
2 Make the network balanced, i.e.,:



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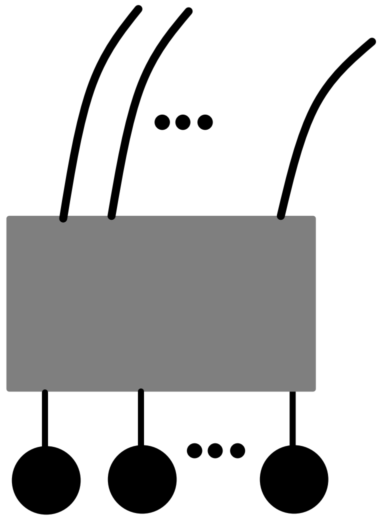

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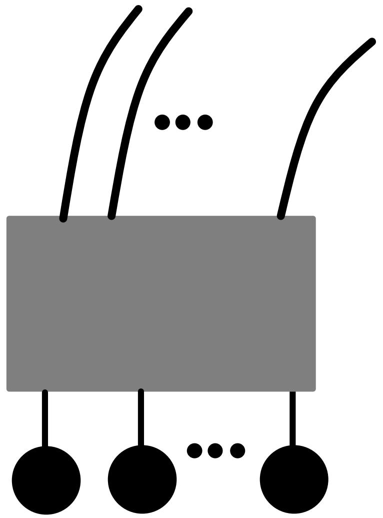
$$local\ uplink\ load = number\ of\ endpoints$$



DESIGNING AN EFFICIENT NETWORK TOPOLOGY

ATTACHING ENDPOINTS: DIAMETER 2

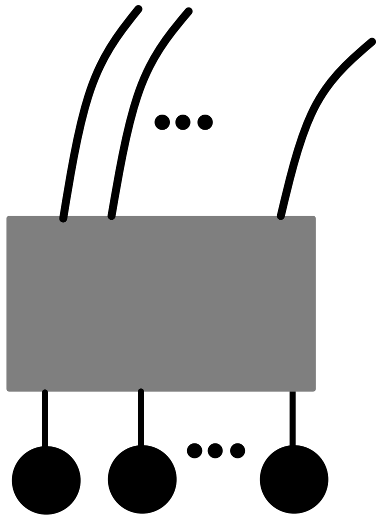
1 Get load *l* per router-router channel (average number of routes per channel)

$$l = \frac{total\ number\ of\ routes}{total\ number\ of\ channels}$$

2 Make the network balanced, i.e.,:

each endpoint can inject at full capacity

$$local\ uplink\ load = number\ of\ endpoints\ = l$$



Designing An Efficient Network Topology

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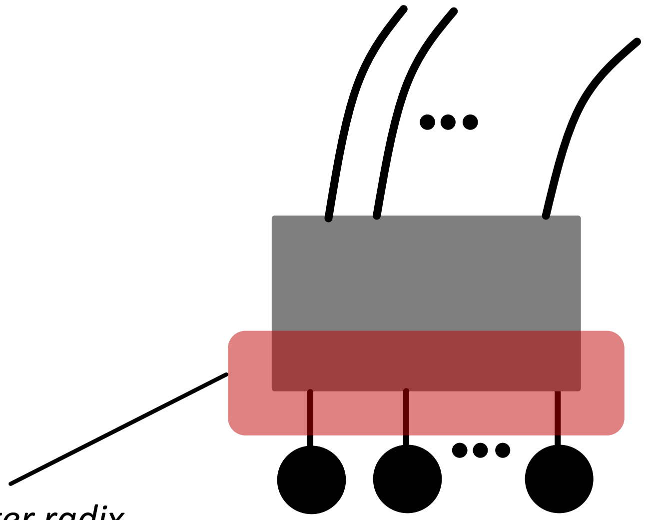

concentration = 33% of router radix

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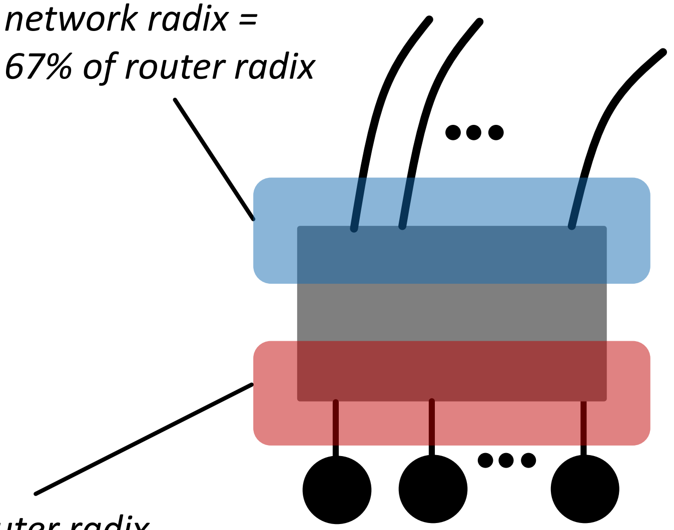
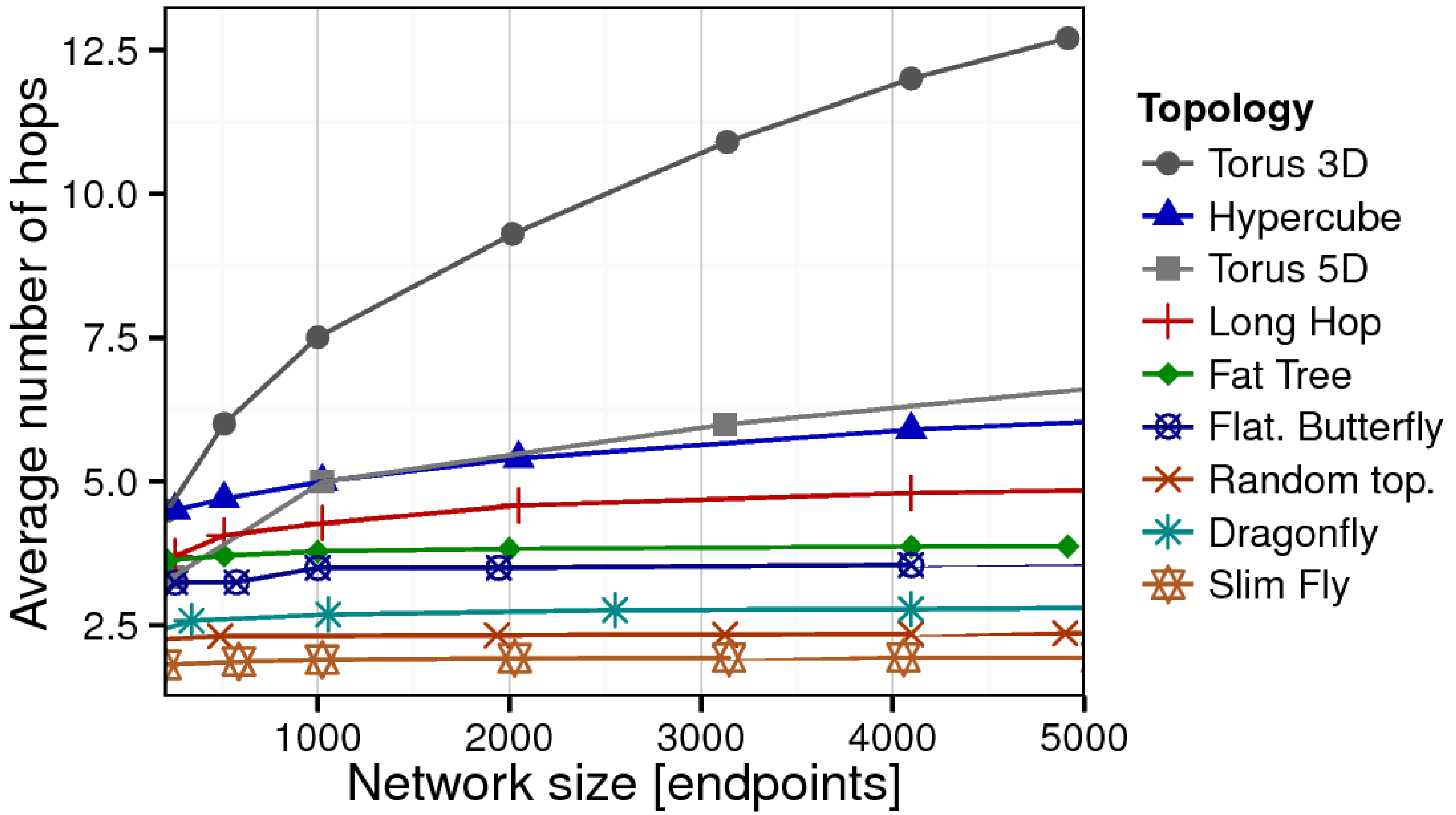


Structure Analysis

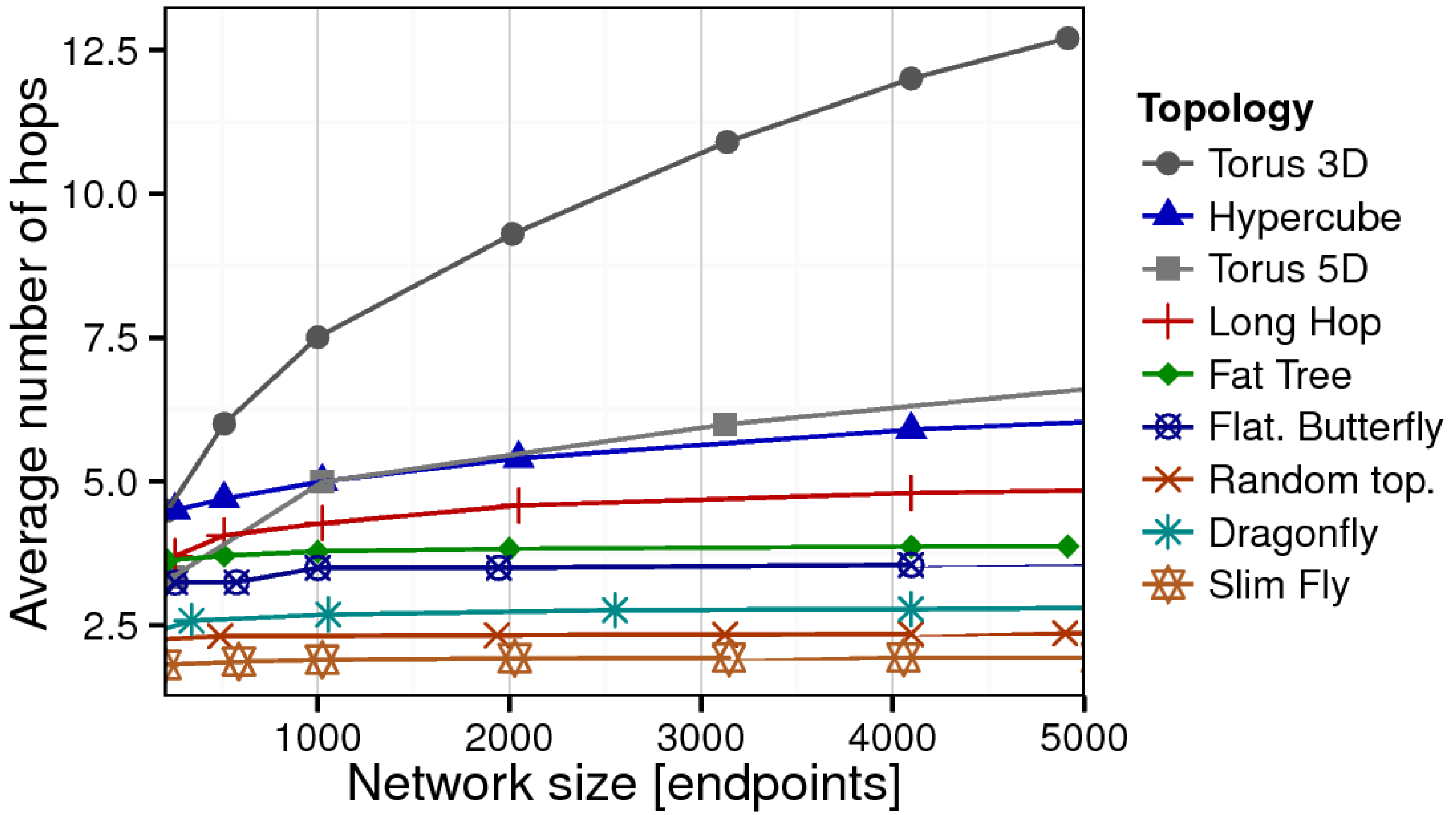
Average Distance



Structure Analysis

Average Distance

Uniform random traffic
using minimum path routing



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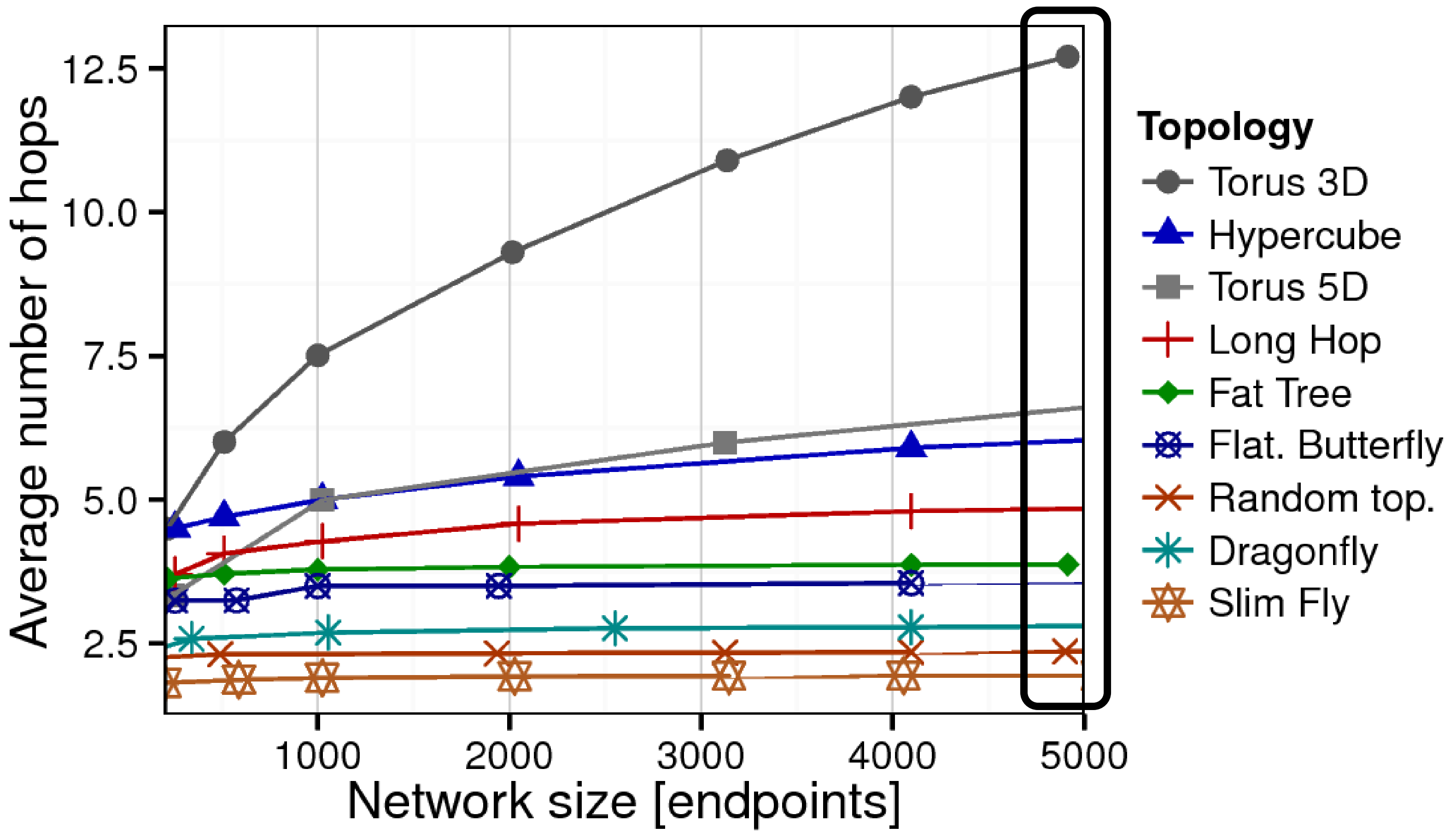
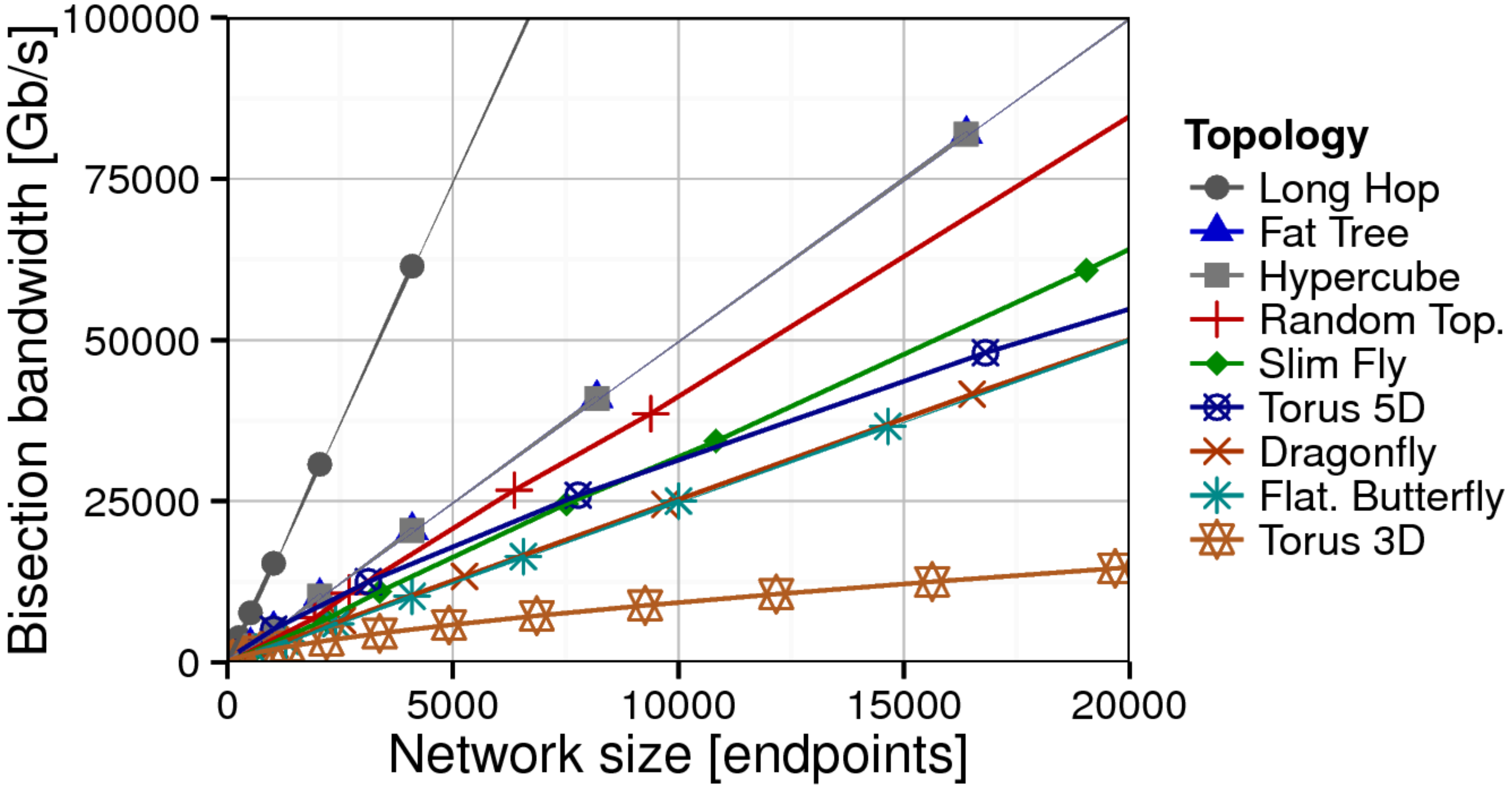


Structure Analysis

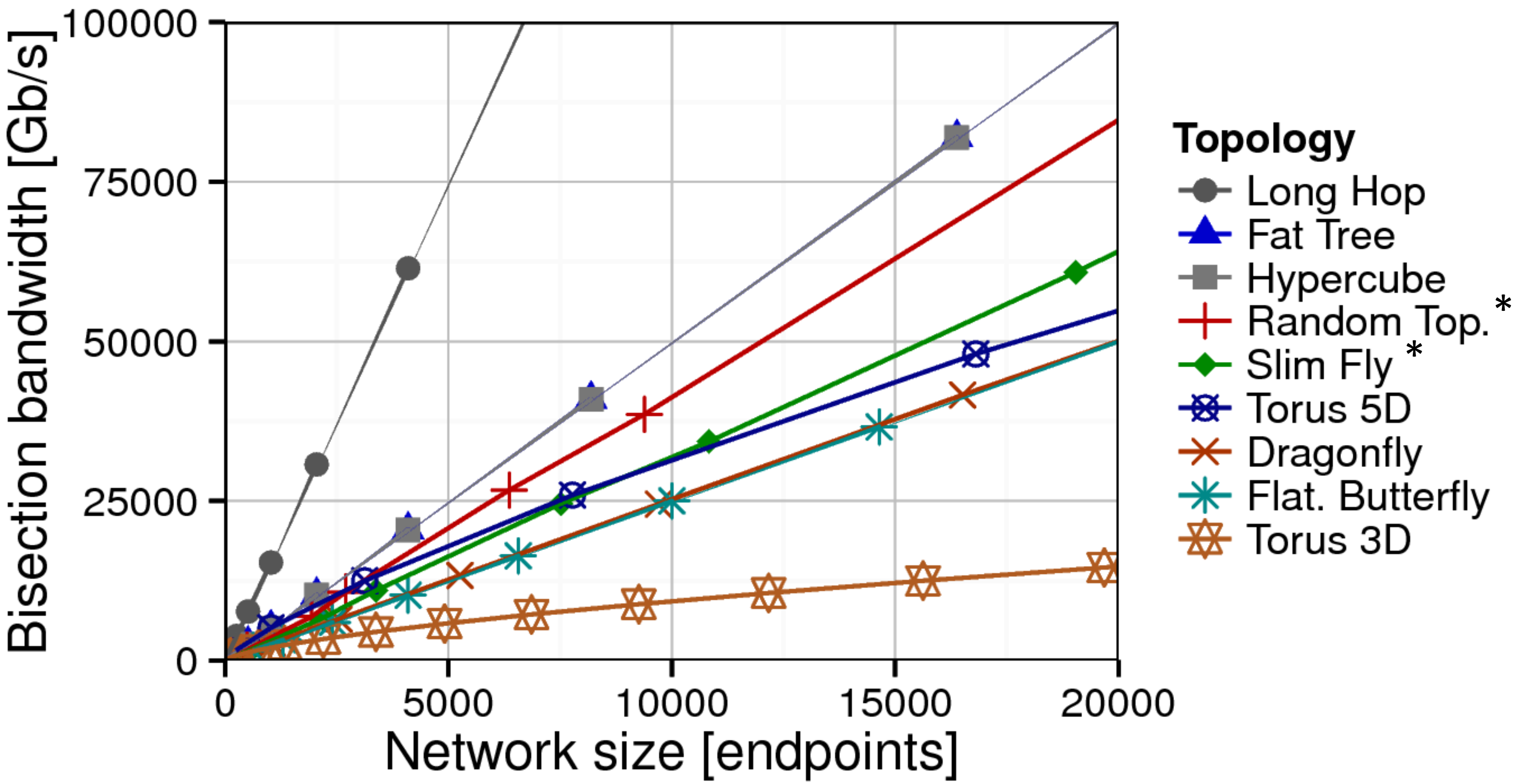
Bisection Bandwidth (BB)



Structure Analysis

Bisection Bandwidth (BB)

*BB approximated with the Metis partitioner [1]

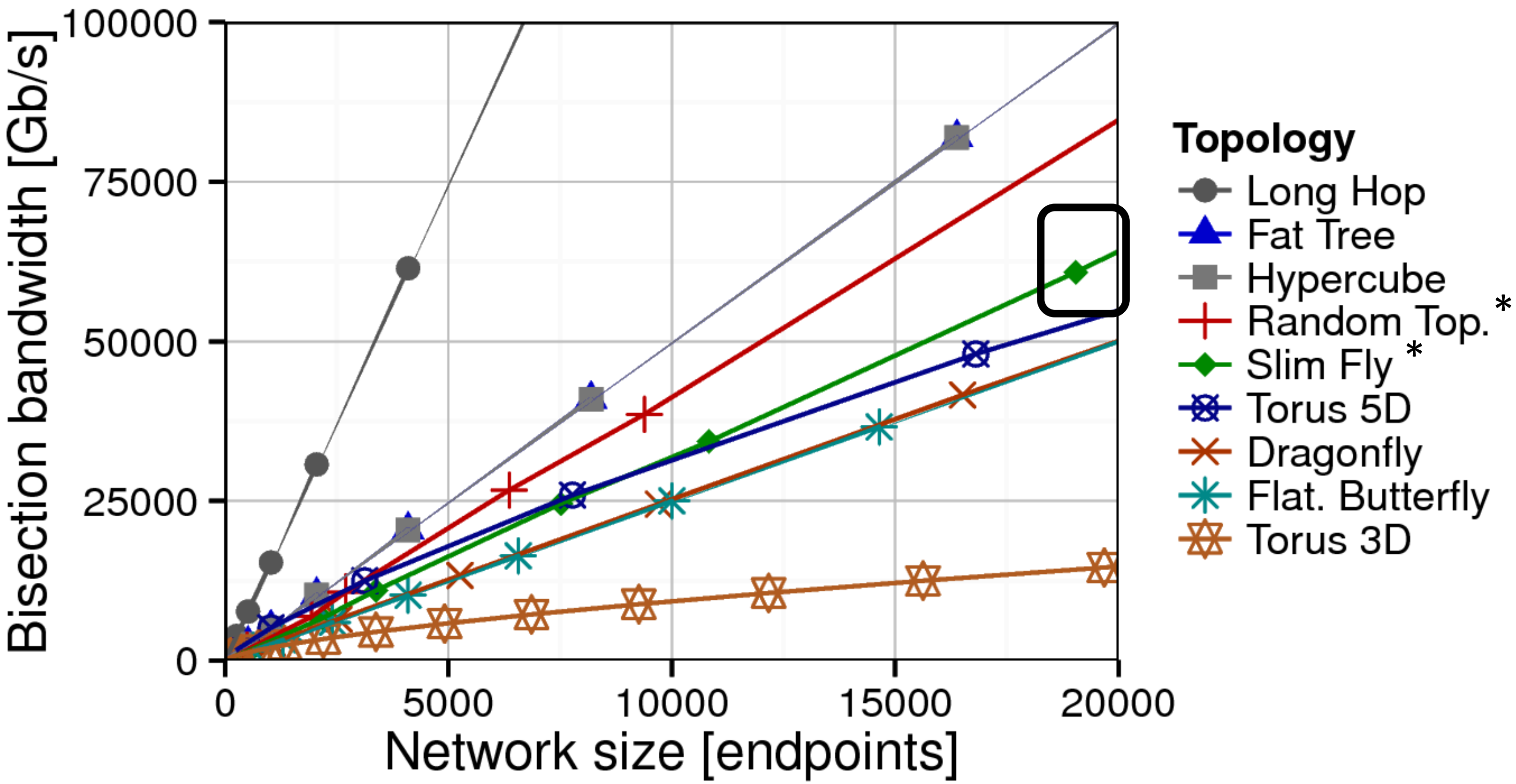


[1] G. Karypis, V. Kumar. A fast and high quality multilevel scheme for partitioning irregular graphs. ICPP'95

STRUCTURE ANALYSIS

BISECTION BANDWIDTH (BB)

*BB approximated with the Metis partitioner [1]



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